



SANTHIRAM ENGINEERING COLLEGE (AUTONOMOUS)

Approved by A.I.C.T.E., New Delhi, Permanently Affiliated to JNT University, Ananthapuramu;
Accredited by NAAC with Grade-A, Accredited by NBA (ECE & CSE);
An ISO 9001:2015 Certified Institution, 2(f) & 12(B) recognition by UGC Act, 1956
NH-40, Nandyal-518501, Nandyal (Dist), A.P.

Learn-Grow-Empower

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.TECH (ECE-VLSI SD)

REGULAR TWO YEAR PG DEGREE COURSE
(Applicable for the Admitted Batch 2025-26)

REGULATIONS: R-25





SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

Program Educational Objectives (PEOs)

Graduates of the M. Tech in VLSI System Design program will be able to:

- **PEO1:** Identify and apply appropriate Electronic Design Automation software and electronic equipment to analyze, synthesize and evaluate to solve real world problems in the VLSI domain to create innovative products and systems.
- **PEO2:** Pursue research studies in the core or allied areas of VLSI circuits and systems.
- **PEO3:** Inculcate Positive Attitude, professional ethics, effective Communication, and interpersonal skills to succeed in the profession exhibiting through research and development both as a team member and leader.

Program Specific Outcomes (PSOs)

Graduates of the M. Tech in VLSI System Design program will be able to:

- **PSO1:** Ability to design and integrate analog, digital and mixed signal circuits, and systems.
- **PSO2:** Design and develop solutions for real-world problems in the domain of IC fabrication, testing, verification, and prototype development focusing on applications.
- **PSO3:** Understand, analyze, design and simulate the various communication systems, data processing techniques and validate their performance for practical applications.

PROGRAM OUTCOMES (POs)

- **PO1:** An ability to independently carry out research, investigation and development work to solve practical problems.
- **PO2:** An ability to write and present a substantial technical report/document.
- **PO3:** Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements of the appropriate bachelor program.



SANTHIRAM ENGINEERING COLLEGE: NANDYAL

ACADEMIC RULES & REGULATIONS

(Effective for the students admitted into I year from the Academic Year 2025-2026)

Santhiram Engineering College, Nandyal (SREC) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M. Tech) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Santhiram Engineering College, Nandyal (SREC) shall confer M. Tech degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. Award of the M. Tech Degree

A student will be declared eligible for the award of the M. Tech degree if he/she fulfils the following:

- 1.1 Pursues a course of study for not less than two academic years and not more than four academic years.
- 1.2 Registers for 75 credits and secures all 75 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M. Tech course and their admission stands cancelled.

3. Programme of Study:

The following M. Tech Specializations are offered at present in different branches of Engineering and Technology in non-autonomous affiliated colleges:

S. No.	Discipline	Name of the Specialization	Code
01	Electronics and Communication Engineering	Embedded Systems	55
		VLSI System Design	57
02	Computer Science and Engineering	Computer Science & Engineering	58
		CSE (Artificial Intelligence & Machine Learning)	13

4. Eligibility for Admissions:

- 4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.
- 4.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECE) for M. Tech programmes an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. Programme related terms:

- 5.1 **Credit:** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week. Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

- 5.2 **Academic Year:** Two consecutive (one odd + one even) semesters constitute one academic year.
- 5.3 **Choice Based Credit System (CBCS):** The CBCS provides choice for students to select from the prescribed courses.

6. Programme Pattern:

- 6.1 Total duration of the of M. Tech programme is two academic years
- 6.2 Each academic year of study is divided into two semesters.
- 6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.
- 6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech programme.
- 6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.
- 6.6 All subjects/courses offered for the M. Tech degree programme are broadly classified as follows:

S. No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/department/branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Mandatory Course	Quantum Technology and Application Research methodology & IPR	To understand importance of latest technologies, research and process of creation of patents through research
4.		Skill Enhancement courses (SE)	Interdisciplinary / job-oriented/domain courses which are relevant to the industry
		Comprehensive Viva	To test the overall domain knowledge
		Short Term Industry Internship	To provide real time exposure
		Dissertation	To provide application of domain knowledge to solve real problems
5.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners.

- 6.7 The college shall take measures to implement Virtual Labs (<https://www.vlab.co.in>) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.
- 6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.
- 6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

- 7.1 A student shall be eligible to appear for the external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.
- 7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.
- 7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence
- 7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.
- 7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.
- 7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.
- 7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.
- 7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

- 8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.
- 8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction period. The other 10 marks is awarded for continuous assessment in the form of assignments, quizzes, open book examination, presentation, etc. First mid examination shall be conducted for I & II units of the syllabus and second mid

examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) and each question carries 10 marks. Final Internal marks for a total of 40 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other.

- 8.3 The following pattern shall be followed in the End Examination:
- Five questions shall be set from each of the five units with either/or type for 12 marks each.
 - All the questions have to be answered compulsorily.
 - Each question may consist of one, two or more bits.
- 8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance. The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15.
- 8.5 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re- examination shall be conducted for failed candidates for 40 marks for every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.
- 8.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.
- 8.7 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.
- 8.8 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the Institution norms and shall be produced to the Committees of the University as and when the same are asked for.

9. Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the Institution shall allow up to a maximum of 40% of the Professional and Open Electives in a semester through SWAYAM/SWAYAM Plus.

- 9.1 The Institution shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.
- 9.2 The student has to register at least any one elective course and complete the course through MOOCs for credit transfer and award the degree.

- 9.3 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform
- 9.4 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution
- 9.5 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.
- 9.6 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.
- 9.7 Students may register for an 8-week (2 credits) or 12-week (3 credits) SWAYAM / SWAYAM plus course with the approval of the Head of the Department (HOD).
- 9.8 Examination fees, if applicable, shall be borne by the student. Pass marks and grading will be as per the Institution academic regulations.
- 9.9 A student must get minimum 40% marks for assignments and quizzes on the SWAYAM/ SWAYAM plus platform to be eligible for the end-semester examination. The students who are unable to get minimum internal marks in SWAYAM/ SWAYAM plus platform, they have to re-register for the course in subsequent semester through SWAYAM/ SWAYAM plus platform.
- 9.10 The end-semester exam may be conducted by the National Testing Agency (NTA), the National Programme on Technology Enhanced Learning (NPTEL) or the Institution during the regular end-term exams. Evaluation shall comprise 60% weightage for the end-semester examination and 40% for assignments and quizzes conducted by the SWAYAM/ SWAYAM plus course coordinator. The student has to get 50% marks for internal and external with minimum of 40% marks in the external examination to declare them as pass.
- 9.11 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester. However, the credits will be transferred to the students who got minimum 50% marks with 40% marks in the external examination
- 9.12 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.
- 9.13 The Institution shall ensure no overlap of SWAYAM MOOC exams with that of the Institution examination schedule. In case of delay in SWAYAM results, the Institution will re-issue the marks sheet for such students.
- 9.14 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the minimum 50% of marks and grades.
- 9.15 The respective Departments shall submit the following to the examination section of the Institution:
 - i. List of students who have passed MOOC courses in the current semester along with the certificates of completion.
 - ii. Undertaking form filled by the students for credit transfer.
- 9.16 The Institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only

after seeking approval of the Institution/University at least three months prior to the commencement of the semester.

10. Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

- 10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.
- 10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.
- 10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.
- 10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.
- 10.5 For each theory subject, the candidate has to pay the requisite fee along with the requisition through concerned Head of the department.
- 10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Progress of the project work is monitored through three reviews:

- Project review – I at the beginning of the III semester for zero marks
- Project review – II at the end of the third semester for 100 marks
- Project review – III before submission of the thesis i.e., end of the IV semesters for 100 marks

External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the

M. Tech programme.

- 11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).
- 11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.
- 11.3 Project work shall be carried out under the supervision of teacher in the parent department concerned.
- 11.4 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases, one

of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

- 11.5 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.
- 11.6 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.
- 11.7 After registration, a candidate must present in Project Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.
- 11.8 The Project Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.
- 11.9 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - II. Only after successful completion of Project Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Review - II shall reappear after three months.
- 11.10 The Project Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - III. If student fails to obtain the required minimum marks, he/she has to reappear for Project Review - III after a month.
- 11.11 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.
- 11.12 After approval from the PRC, the student is permitted to submit a report. The dissertation report will be accepted only when the plagiarism is within 30% checked through Turnitin software (repository mode). The plagiarism report shall be submitted along with the dissertation report.
- 11.13 Research paper related to the Project Work shall be published in an SCI/ESCI/Scopus/UGC Care listed journal, or in conference proceedings with ISBN number organized by professional societies such as IEEE, IET, etc.
- 11.14 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.
- 11.15 The dissertation shall be adjudicated by an external examiner selected by the Institution. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each student. However, the dissertation will be adjudicated by one examiner nominated by the Head of the Institution.

- 11.16 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after the approval from the Institution.
- 11.17 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.
- 11.18 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.
- 11.19 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12. Industry Internships:

Industry internship either onsite or virtual with a minimum of 06-08 weeks" duration, done at the end of 1st year second semester. It shall be completed in collaboration with local industries, Govt. Organizations, construction agencies, Power projects, software MNCs or any industries in the areas of concerned specialization of the PG program. The student shall register for the internship as per course structure after commencement of academic year.

Evaluation of the summer internships shall be through the departmental committee. A student will be required to submit a summer internship report to the concerned department and appear for an oral presentation before the departmental committee comprising of Head of the Department, Mentor/Supervisor of the internship and a senior faculty member of the department. A certificate of successful completion from industry shall be included in the report. Internship will be evaluated for 100 marks with 50 marks for the report evaluated by the mentor and 50 marks for oral presentation. A student should secure minimum 50% of marks for successful completion. In case, if a student fails, he/she shall reappear as and when semester supplementary examinations are conducted by the Institution.

13. Comprehensive Viva

A Comprehensive Viva shall be conducted after the II Semester examinations for 100 marks by a committee consisting of the Head of the Department, one senior faculty member of the same specialization, and an external subject expert appointed by the Head of the Institution. The student must secure a minimum of 50% marks to be declared as passed

14. Credits for Co-curricular Activities

The college shall be introducing Co-Curricular activities in III semester with One credit. The student must be participating in Co-Curricular / extra-curricular activities such as publishing a paper or participating in a National / International workshops / symposium / seminar / training organized by any private institution / Govt. organization / Training centers in virtual/offline mode. The student has to participate in Co-Curricular activities during their program duration and submit the certificate at the end of the III semester. If he/she fails to submit will not be eligible for the award of degree. In such cases, the student shall repeat and submit the Co-Curricular activity.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits / Activity
Participation in National Level Seminar/ Conference / Workshop / Training programs (related to the specialization of the student)	0.5
Participation in International Level Seminar / Conference / workshop/ Training programs held outside India (related to the specialization of the student)	1
Academic Award/Research Award from State Level/National Agencies	0.5
Academic Award/Research Award from International Agencies	1
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	0.5
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	1

Note:

- Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit. A minimum participation of five days is required to earn the necessary credits. Alternatively, the student may attend five different one day programs to meet this requirement.
- Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.
- Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

15. Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed: After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
$\geq 80 < 90$	A (Excellent)	9
$\geq 70 < 80$	B (Very Good)	8
$\geq 60 < 70$	C (Good)	7
$\geq 50 < 60$	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

- A student obtaining Grade „F“ or Grade „Ab“ in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.
- For noncredit audit courses, “Satisfactory” or “Unsatisfactory” shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i) / \Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

- i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i) / \Sigma C_i$$

where " S_i " is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

- ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale.

Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

16. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	CGPA to be secured
First Class with Distinction	≥ 7.5
First Class	$7.5 > CGPA \geq 6.5$
Pass Class	$CGPA < 6.5$

17. Exit Policy:

The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

18. Withholding of Results:

If the candidate has any case of in-discipline pending against him/her, the result of the candidate shall be withheld, and he/she will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

19. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

20. General:

- 20.1 The academic regulations should be read as a whole for purpose of any interpretation.
- 20.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.
- 20.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.
- 20.4 Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.
- 20.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.
- 20.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	<i>If the candidate:</i>	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and handed over to the examination of the autonomous college.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all examinations, if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider; he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations / Assistant Controller of Examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ Controller of Examinations / Assistant Controller of Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
3. A show cause notice shall be issued to the college.
4. Impose a suitable fine on the college.
5. Shifting the examination centre from the college to another college for a specific period of not less than one year.

Note: -

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.



M. Tech (VLSISD Branch) Course Structure

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN****M.Tech. I Sem. - Course Structure**

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week			
				L	T	P	C
1	25D57101	PC	CMOS ANALOG IC DESIGN	3	0	0	3
2	25D57102	MC(C)	CMOS DIGITAL IC DESIGN	3	0	0	3
3	25D57103A	PE	CAD FOR VLSI (PE-I)	3	0	0	3
4	25D57103B	PE	MICROCHIP FABRICATION TECHNIQUES (PE-I)	3	0	0	3
5	25D57103C	PE	SCRIPTING LANGUAGES FOR VLSI (PE-I)	3	0	0	3
6	25D57103D	PE	NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)	2	0	0	3
7	25D57103E	PE	MEMS AND NEMS (PE-I)	3	0	0	3
8	25D57104A	PE	ASIC DESIGN (PE-II)	3	0	0	3
9	25D57104B	PE	FPGA ARCHITECTURES AND APPLICATIONS (PE-II)	3	0	0	3
10	25D57104C	PE	DEEP LEARNING FOR VLSI (PE-II)	3	0	0	3
11	25D57104D	PE	DEVICE MODELLING (PE-II)	3	0	0	3
12	25D57104E	PE	MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)	3	0	0	3
13	25D57105	PC	CMOS ANALOG IC DESIGN LAB	0	0	4	2
14	25D57106	PC	CMOS DIGITAL IC DESIGN LAB	0	0	4	2
15	25D57107	MC(C)	RESEARCH METHODOLOGY AND IPR	2	0	0	2
16	25D57108	SC	RTL SYNTHESIS, SIMULATION AND VERIFICATION	0	1	2	2
17	25D57109A	MC(NC)	ENGLISH FOR RESEARCH PAPER WRITING (AC-I)	2	0	0	0
18	25D57109B	MC(NC)	VALUE EDUCATION (AC-I)	2	0	0	0
19	25D57109C	MC(NC)	DISASTER MANAGEMENT (AC-I)	2	0	0	0
20	25D57109D	MC(NC)	ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)	2	0	0	0

M.Tech. II Sem. - Course Structure

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week			
				L	T	P	C
1	25D57201	PC	CMOS MIXED SIGNAL IC DESIGN	3	0	0	3
2	25D57202	PC	PHYSICAL DESIGN AUTOMATION	3	0	0	3
3	25D57203A	PE	DIGITAL VLSI TESTING (PE-III)	3	0	0	3
4	25D57203B	PE	INTEGRATED CIRCUITS, MOSFETS, OP-AMPS AND THEIR APPLICATIONS (PE-III)	3	0	0	3
5	25D57203C	PE	SOC TESTING AND VERIFICATION (PE-III)	3	0	0	3
6	25D57203D	PE	SEMICONDUCTOR MEMORY DESIGN AND TESTING (PE-III)	3	0	0	3
7	25D57203E	PE	ADVANCED VLSI INTERCONNECTS (PE-III)	3	0	0	3
8	25D57204A	PE	SEMICONDUCTOR DEVICES FOR NEXT GENERATION FETS: A PHYSICS PERSPECTIVE (PE-IV)	3	0	0	3
9	25D57204B	PE	DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS(PE-IV)	3	0	0	3
10	25D57204C	PE	ALGORITHMS FOR VLSI DESIGN (PE-IV)	3	0	0	3
11	25D57204D	PE	LOW POWER VLSI DESIGN (PE-IV)	3	0	0	2
12	25D57204E	PE	VLSI SIGNAL PROCESSING (PE-IV)	3	0	0	2
13	25D57205	PC	CMOS MIXED SIGNAL IC DESIGN LAB	0	0	4	2
14	25D57206	PC	PHYSICAL DESIGN AUTOMATION LAB	0	0	4	2
15	25D57207	MC(C)	QUANTUM TECHNOLOGIES AND APPLICATIONS	2	0	0	2
16	25D57209A	PE	ENTREPRENEURSHIP ESSENTIALS (AC-II)	2	0	0	0
17	25D57209B	PE	PEDAGOGY STUDIES (AC-II)	2	0	0	0
18	25D57209C	PE	YOGA FOR STRESS MANAGEMENT (AC-II)	2	0	0	0
19	25D57209D	MC(NC)	CONSTITUTION OF INDIA (AC-II)	2	0	0	0
20	25D57208	PR	COMPREHENSIVE VIVA VOCE	0	0	0	2

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN****M.Tech. III Sem. - Course Structure**

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week			
				L	T	P	C
1	25D57301A	PE	BI-CMOS TECHNOLOGY AND APPLICATIONS (PE-V)	3	0	0	3
2	25D57301B	PE	OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN (PE-V)	3	0	0	3
3	25D57301C	PE	VLSI DESIGN FLOW- RTL TO GDS (PE-V)	3	0	0	3
4	25D57301D	PE	SOC ARCHITECTURE (PE-V)	3	0	0	3
5	25D06301	OE	IOT AND ITS APPLICATIONS (OE-I)	3	0	0	3
6	25D20301	OE	GREEN BUILDINGS (OE-I)	3	0	0	3
7	25D93301	OE	ROAD SAFETY ENGINEERING (OE-I)	3	0	0	3
8	25D91301	OE	INDUSTRIAL SAFETY (OE-I)	3	0	0	3
9	25D58101	OE	ADVANCED DATA STRUCTURES & ALGORITHMS(OE-I)	3	0	0	3
10	25D58305	OE	CLOUD COMPUTING (OE-I)	3	0	0	3
11	25D13305	OE	AI TOOLS (OE-I)	3	0	0	3
12	25D95301	OE	PHOTOVOLTAIC SYSTEMS (OE-I)	3	0	0	3
13	25D15301	OE	INTEGRATED PRODUCT DESIGN AND DEVELOPMENT (OE-I)	3	0	0	3
14	25D99301A	OE	ADVANCED NUMERICAL METHODS AND COMPUTATIONAL MATHEMATICS (OE-I)	3	0	0	3
15	25D99301B	OE	MATHEMATICS FOR MACHINE LEARNING AND DATA SCIENCE (OE-I)	3	0	0	3
16	25D99301C	OE	STATISTICAL LEARNING THEORY AND MATHEMATICAL FOUNDATIONS OF AI (OE-I)	3	0	0	3
17	25D99301D	OE	CHEMISTRY OF NANOMATERIALS AND APPLICATIONS IN ENGINEERING (OE-I)	3	0	0	3
18	25D99301E	OE	PHOTONICS FOR ENGINEERS (OE-I)	3	0	0	3
19	25D57302	PR	DISSERTATION PHASE – I	0	0	20	10
20	25D57303	PR	INDUSTRY INTERNSHIP	0	0	0	2
21	25D57304	PR	CO- CURRICULAR ACTIVITIES	0	0	0	1

M.Tech. IV Sem. - Course Structure

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week			
				L	T	P	C
1	25D57401	PR	DISSERTATION PHASE-II	0	0	32	16



**M. Tech (VLSISD Branch)
I-Semester
Course Structure**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN****M.Tech. I Sem. - Course Structure**

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				L	T	P	C	IM	EM	Total
1	25D57101	PC	CMOS ANALOG IC DESIGN	3	0	0	3	40	60	100
2	25D57102	MC(C)	CMOS DIGITAL IC DESIGN	3	0	0	3	40	60	100
3	25D57103A	PE	CAD FOR VLSI (PE-I)	3	0	0	3	40	60	100
4	25D57103B	PE	MICROCHIP FABRICATION TECHNIQUES (PE-I)	3	0	0	3	40	60	100
5	25D57103C	PE	SCRIPTING LANGUAGES FOR VLSI (PE-I)	3	0	0	3	40	60	100
6	25D57103D	PE	NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)	2	0	0	3	40	60	100
7	25D57103E	PE	MEMS AND NEMS (PE-I)	3	0	0	3	40	60	100
8	25D57104A	PE	ASIC DESIGN (PE-II)	3	0	0	3	40	60	100
9	25D57104B	PE	FPGA ARCHITECTURES AND APPLICATIONS (PE-II)	3	0	0	3	40	60	100
10	25D57104C	PE	DEEP LEARNING FOR VLSI (PE-II)	3	0	0	3	40	60	100
11	25D57104D	PE	DEVICE MODELLING (PE-II)	3	0	0	3	40	60	100
12	25D57104E	PE	MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)	3	0	0	3	40	60	100
13	25D57105	PC	CMOS ANALOG IC DESIGN LAB	0	0	4	2	40	60	100
14	25D57106	PC	CMOS DIGITAL IC DESIGN LAB	0	0	4	2	40	60	100
15	25D57107	MC(C)	RESEARCH METHODOLOGY AND IPR	2	0	0	2	40	60	100
16	25D57108	SC	RTL SYNTHESIS, SIMULATION AND VERIFICATION	0	1	2	2	40	60	100
17	25D57109A	MC(NC)	ENGLISH FOR RESEARCH PAPER WRITING (AC-I)	2	0	0	0	40	0	40
18	25D57109B	MC(NC)	VALUE EDUCATION (AC-I)	2	0	0	0	40	0	40
19	25D57109C	MC(NC)	DISASTER MANAGEMENT (AC-I)	2	0	0	0	40	0	40
20	25D57109D	MC(NC)	ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)	2	0	0	0	40	0	40



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M. Tech (VLSISD Branch) I-Semester Syllabus

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57101) CMOS ANALOG IC DESIGN

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I MOS DEVICES AND MODELING**

The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling -Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II ANALOG CMOS SUB-CIRCUITS

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage Band gap Reference.

UNIT-III CMOS AMPLIFIERS

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

UNIT-IV CMOS OPERATIONAL AMPLIFIERS

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT-V COMPARATORS

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce.
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Understand significance of different biasing styles and apply them for designing analog ICs.
2. Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
3. Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57102) CMOS DIGITAL IC DESIGN

Course Category	Mandatory Course (credit)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

UNIT-I MOS DESIGN PSEUDO NMOS LOGIC

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III SEQUENTIAL MOS LOGIC CIRCUITS

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

COURSE OUTCOMES:

1. Design CMOS inverters with specified noise margins and propagation
2. Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
3. Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
4. Design basic combinational and sequential elements using NMOS and CMOS design strategies.
5. Analyze the dynamic performance of CMOS circuits

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103A) CAD FOR VLSI (PE-I)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I INTRODUCTION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II PARTITIONING

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing

UNIT-III FLOOR PLANNING

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV PLACEMENT AND ROUTING & GLOBAL ROUTING AND DETAILED ROUTING

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms. Global Routing–Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing–Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing–Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

COURSE OUTCOMES:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement
3. Optimize the implemented design for area, timing and power by applying suitable constraints.
4. Practice the application of fundamentals of VLSI technologies
5. Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103B) MICROCHIP FABRICATION TECHNIQUES (PE-I)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Comprehend impact of semiconductor industry on the design of development of integrated circuits.
2. Acquaint with clean room technology
3. Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
4. Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
5. Understand packaging principles

UNIT-I INTRODUCTION TO PROCESSING

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction

UNIT-II PHOTOLITHOGRAPHY

Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT-III DIFFUSION & ION IMPLANTATION

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT-IV FILM DEPOSITIONS AND GROWTH

Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT-V YIELD

Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors. Packaging: Chip characteristics, package functions, package operations



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

COURSE OUTCOMES:

1. Understand various stages of fabrication
2. Understand various packaging techniques and Design rules
3. Understand the aspects of diffusion, ion implantation techniques.
4. Classify various thin films and its characteristics.
5. Specify NMOS and CMOS design rules corresponding to package operations.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103C) SCRIPTING LANGUAGES FOR VLSI (PE-I)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To learn the fundamental syntax, control structures, file I/O, and data processing capabilities of PERL, TCL, and Python.
2. To apply Regular Expressions: Implement regular expressions in scripts to effectively parse and extract specific data from complex EDA tool reports and log files.
3. To automate EDA Tool Flow: Write scripts to control and automate EDA tools, managing workflows for simulation, synthesis, and other design-cycle tasks.
4. To develop VLSI Task Automation: Create efficient automation scripts to handle common VLSI design tasks, such as managing design files, generating reports, and checking for errors.
5. To select Appropriate Tools: Evaluate the requirements of a specific automation task and select the most appropriate scripting language (PERL, TCL, or Python) for the use case.

UNIT-I INTRODUCTION TO SCRIPTING LANGUAGES IN EDA

Introduction to scripting and automation, Scripting vs compiled languages, using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops – overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

UNIT-II PERL SCRIPTING

Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, using files and file handles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

UNIT-III TCL SCRIPTING

Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV PYTHON FOR DESIGN AUTOMATION AND DATA PROCESSING

Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, using os, sys, and subprocess modules, Writing utility scripts for automation

UNIT-V ADVANCED INTEGRATION AND COMPARISON

Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

REFERENCE BOOKS:

1. Robbins, Arnold. Scripting the UNIX System: Using Bash, Perl, and More. Addison-Wesley, 2003. g
2. Ousterhout, John K. Tcl and the Tk Toolkit. 2nd ed., Addison-Wesley Professional, 2009.
3. Python Software Foundation. Python Language Reference Manual. <https://docs.python.org>

COURSE OUTCOMES:

1. Describe the role of scripting languages in EDA workflows and differentiate between scripting and compiled languages.
2. Write PERL scripts to perform text parsing, data extraction, and report generation.
3. Develop TCL scripts to automate tool commands and control design processes in EDA tools.
4. Construct Python scripts for file handling, data processing, and automation of design-related tasks.
5. Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications

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M.Tech. I Sem.

L	T	P	C
2	0	0	3

(25D57103D) NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the basic idea behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and technologies for future applications.
3. To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT-I INTRODUCTION OF NANO MATERIALS AND NANOTECHNOLOGIES

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms – Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive-hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT-II FUNDAMENTALS OF NANOMATERIALS

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT-III MICRO-AND NANOLITHOGRAPHY TECHNIQUES

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT-IV INTRODUCTION & SYNTHESIS OF CNTS-ARC-DISCHARGE

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs

UNIT-V FERROELECTRIC MATERIALS

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2nd edition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B.S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGrawHill Education 2012.

REFERENCE BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011
2. Digital Integrated Circuits - A Design Perspective, Jan M. Rabaey, Anant Chandrakasan, Borivoje Nikolic, 2nd Edition, PHI

COURSE OUTCOMES:

1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To Understand the advantages and Challenges of MEMS
4. To analyze the synthesis of CNTs with applications.
5. To acquire knowledge on the operation and characterization to achieve precisely designed systems

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103E) MEMS AND NEMS (PE-I)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To introduce Nano-and Microsystems
2. To understand the modeling of micro and nano scale electromechanical systems

UNIT-I INTRODUCTION TO MEMS AND NEMS

MEMS and NEMS definitions, Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Biomimetics, Biological analogies, and design-Biomimetics Fundamentals, Biomimetics for NEMS and MEMS, Nano-ICs and Nano computer architectures

UNIT-II MODELING OF MICRO AND NANO SCALE ELECTROMECHANICAL SYSTEMS

Introduction to modelling, analysis and simulation, basic electro-magnetic with application to MEMS and NEMS, modeling developments of micro-and nano actuators using electromagnetic-Lumped-parameter mathematical models of MEMS, energy conversion in NEMS and MEMS

UNIT-III MEMS FABRICATION TECHNOLOGIES

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching.

UNIT-IV MICROMACHINING

Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT-V NANOSYSTEMS AND QUANTUM MECHANICS

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TEXT BOOKS:

1. Sergey Edward Lyshevski, Lyshevski Edward Lyshevski, Nano-Electro Mechanical and Micro-Electro Mechanical Systems, Fundamental of Nano-and Micro-Engineering 2005, 2nd Ed., CRC Press.
2. A. S. Edelstein and Cammarata, Nanomaterials: Synthesis, Properties and Applications, 2002, Institute of Physics, Bristol, Philadelphia



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Kalantar-Zadeh K, Nanotechnology Enabled Sensors, 2008, Springer.
2. Serge Luryi, Jimmy Xu, Alex Zaslavsky, Future trends in MicroElectronics, 2007, John Wiley & Sons, Inc. Hoboken, New Jersey

e-Resources and Digital Material:

1. https://onlinecourses.nptel.ac.in/noc22_ee36/preview

COURSE OUTCOMES:

1. Acquire the knowledge of Nano- and Microsystems.
2. Identify the methods of modeling of micro and nano scale electromechanical
3. Ability to design the micro devices, micro systems using the MEMS fabrication process.
4. Gain a knowledge of basic approaches for micromachining
5. Develop experience on micro/nano systems for photonics.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104A) ASIC DESIGN (PE-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand different types of ASICs and their libraries.
2. To understand about programmable ASICs, I/O modules and their interconnects.
3. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT-I INTRODUCTION TO ASICs

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT-II PROGRAMMABLE ASICs AND PROGRAMMABLE ASIC LOGIC CELLS

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT-IV LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT-V SIMULATION, TEST AND ASIC CONSTRUCTION

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

REFERENCE BOOKS:

1. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001

COURSE OUTCOMES:

1. Understand different types of ASICs and their libraries.
2. Understand about programmable ASICs, I/O modules and their interconnects.
3. Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.
4. Understand the various Low Level Design Entry and Logic Synthesis
5. Analyze and Simulate the various Tests and ASIC Construction.

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M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104B) FPGA ARCHITECTURES AND APPLICATIONS (PE-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To acquire knowledge about various architectures and device technologies of PLD's
2. To comprehend FPGA Architectures
3. To analyze System level Design and their application for Combinational and Sequential Circuits
4. To familiarize with Anti-Fuse Programmed FPGAs
5. To apply knowledge of this subject for various design applications
6. To familiarize with SRAM FPGAs

UNIT-I INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III SRAM PROGRAMMABLE FPGA

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures

UNIT-IV ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT-V DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Field Programmable Gate Arrays-John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

e-Resources and Digital Material:

1. <http://www.digimat.in/nptel/courses/video/117108040/L01.html>
2. <https://www.youtube.com/watch?v=gCAYY0fHPq4>

COURSE OUTCOMES:

1. Acquire knowledge about various architectures and device technologies of PLD"s
2. Comprehend FPGA Architectures
3. Analyze System level Design and their applications for various architectures.
4. Familiarize with Anti-Fuse Programmed FPGAs
5. Apply knowledge of this subject for various design applications.
6. Familiarize with SRAM FPGAs

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M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104C) DEEP LEARNING FOR VLSI (PE-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To impart knowledge about the Artificial Neural networks and deep learning.
2. To introduce the fundamental concepts relevant to ANN architectures and deep learning algorithms.
3. To understand the applications and use cases of Deep Learning architectures for VLSI circuits and design automation.

UNIT-I INTRODUCTION TO DEEP LEARNING

History and evolution of Deep Learning; Fundamentals of Deep Learning; Training Deep Architectures; Intermediate Representations-Sharing Features and Abstractions across Tasks; Sigmoid Neurons; Gradient Descent; Feedforward Neural Networks; Dropout; Backpropagation – concepts and implementation.

UNIT-II DEEP LEARNING WITH TENSORFLOW

Introduction to Deep Learning and TensorFlow; How Deep Learning Works; Principal Component Analysis (PCA) and its Interpretations; Singular Value Decomposition (SVD); Greedy Layer-wise Pre-training; Improved Activation Functions; Weight Initialization Methods; Batch Normalization; Implementing Basic Deep Learning Models using TensorFlow.

UNIT-III DEEP LEARNING ALGORITHMS AND OPTIMIZATION

Gradient Descent and Backpropagation Techniques; Improving Deep Networks; Multi-Layer Neural Networks; The Challenge of Training Deep Neural Networks; Deep Generative Architectures; Mini-batches and Optimization Techniques; Handling Unstable Gradients; Regularization and Avoiding Over-fitting; Applying Deep Network Theory to Code Implementations.

UNIT-IV ADVANCED DEEP ARCHITECTURES

Introduction to Convolutional Neural Networks (CNNs) for Visual Recognition; Recurrent Neural Networks (RNNs); RNNs in Practice; Long Short-Term Memory (LSTM) and Gated Recurrent Unit (GRU) Architectures; LSTMs and GRUs in Practice; Reinforcement Learning; Importance of Unsupervised Learning; Training Auto encoders.

UNIT-V APPLICATIONS OF DEEP LEARNING IN VLSI

Deep Learning Applications in VLSI Design and Automation – Chip Design, Test Generation, Chip Testing, Diagnosis and Debug, and Characterization; AI-driven Design Flow Automation; Performance Prediction and Optimization in VLSI Circuits using Deep Neural Models.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Deep Learning: Methods and Applications by Li Deng and Dong Yu, now publisher.
2. Neural Networks and Deep Learning by Michael Nielsen, Determination Press.

REFERENCE BOOKS:

1. Hands-On Learning with Scikit-Learn and Tensorflow by Aurelien Geron, Oreilly.
2. Pattern Recognition and Machine Learning by Christopher Bishop, Springer-Verlag Berlin, Heidelberg.
3. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press.

COURSE OUTCOMES:

1. To Describe the key components of AI field and its relation and role in computer science.
2. To Build custom architectures from scratch
3. To be able to apply appropriate architectures for solving, modeling, optimizing and automizing VLSI related options.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

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M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104D) DEVICE MODELLING (PE-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the physics of 2-terminal MOS operation and its characteristics
2. To understand the physics of 4-terminal MOSFET operation and its characteristics.
3. To analyze the SOI MOSFET electrical characteristics.

UNIT-I 2-TERMINAL MOS DEVICE

Threshold voltage modelling (ideal case as well as considering the effects of Q_f , Φ_{ms} and D_{it} .)

UNIT-II C-V CHARACTERISTICS

C-V characteristics (ideal case as well as taking into account the effects of Q_f , Φ_{ms} and D_{it}); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Q_f , Φ_{ms} and D_{it})

UNIT-III 4-TERMINAL MOSFET

Threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT-IV SUB-THRESHOLD CURRENT MODELS

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT-V SOI MOSFET

Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.



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REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009.

COURSE OUTCOMES:

1. Understand the physics of 2-terminal MOS operation and its characteristics
2. Understand the concept of MOS capacitor.
3. Understand the physics of 4-terminal MOSFET operation and its characteristics.
4. To understand Sub threshold current model.
5. Analyze the SOI MOSFET electrical characteristics

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M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104E) MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To introduce the fundamental principles and operation of semiconductor devices used in analog and digital electronic circuits.
2. To develop the ability to analyze and design basic electronic circuits using diodes, BJTs, and MOSFETs.
3. To explain the characteristics and applications of amplifier and switching circuits in both discrete and integrated forms.
4. To provide understanding of frequency response, feedback, and stability aspects in analog circuit design.
5. To enable students to integrate analog and digital concepts for designing mixed-signal electronic systems

UNIT-I TRANSISTOR FUNDAMENTALS AND BASIC CIRCUIT MODELS

Bipolar Junction Transistor; Physical Structure and Modes of operation, Operation in Active Mode, circuit symbols and conventions, BJT as an Amplifier, small circuit model, BJT as a switch and Ebers Moll Model, Simple BJT inverter and Second Order Effects. MOS Transistor Basic, MOS Parasitic & SPICE Model; CMOS Inverter Basics-I

UNIT-II MOS AND BJT AMPLIFIER DESIGN

Power Analysis SPICE Simulation-I, Biasing of MOS Amplifier and its behavior as an analog switch, CMOS CS/CG/SF Amplifier Configuration, Internal cap models and high frequency modelling, JFET, structure and operation. Multistage and Differential Amplifier, Small Signal Operation and Differential Amplifier, MOS Differential Amplifier, BiCMOS Amplifier with Active Load, Multistage Amplifier with SPICE Simulation

UNIT-III FREQUENCY RESPONSE AND FEEDBACK IN AMPLIFIERS

S-domain analysis, transfer function, poles and zeros, High Frequency Response of CS and CE Amplifier, Frequency Response of CC and SF Configuration, Frequency Response of the Differential Amplifier, Cascode Connection and its Operation. General Feedback structure and properties of negative feedback, Basic Feedback Topologies, Design of Feedback Amplifier for all configuration, Stability and Amplifier poles, Bode Plots and Frequency Compensation

UNIT-IV OPERATIONAL AMPLIFIERS AND ANALOG FILTERS

Ideal Operational Amplifier and its terminals, Inverting and Non- Inverting Configuration, As an integrator and Differentiator, Introduction to Analog Computer, Large Signal Operation of Op-Amp and Second order offsets. Butterworth and Chebyshev Filters, First and Second Order Filter Functions, Switched Capacitor based filters, Single-Amplifier Biquadratic Filters, Second Order LCR Resonator.

UNIT-V DIGITAL LOGIC AND SEQUENTIAL CIRCUIT DESIGN

Combinational Logic Design, Sequential Logic Design, Clock Strategies for Sequential Design, Concept of Memory & its Designing



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009.

COURSE OUTCOMES:

1. Explain the working principles of semiconductor devices and their roles in electronic circuits.
2. Analyze the performance of analog and digital circuits using appropriate circuit theorems and models.
3. Design and implement amplifier, oscillator, and switching circuits meeting specified requirements.
4. Evaluate the effects of feedback, frequency response, and biasing on circuit stability and performance.
5. Apply learned concepts to design and simulate discrete and integrated circuits used in practical electronic systems.

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M.Tech. I Sem.

L	T	P	C
0	0	4	2

(25D57105) CMOS ANALOG IC DESIGN LAB

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. To explain the Physical Verification in Layout Design
4. To fully appreciate the design and analyze of analog and mixed signal simulation
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

The students are required to design and implement any TEN Experiments using CMOS 130nm Technology.

The students are required to implement LAYOUTS of any SIX Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using VLSI design tool.
2. Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. Explain the Physical Verification in Layout Design
4. Fully appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
0	0	4	2

(25D57106) CMOS DIGITAL IC DESIGN LAB

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

e-Resources and Digital Material:**COURSE OUTCOMES:**

1. Explain the VLSI Design Methodologies using any VLSI design tool
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Explain the Physical Verification in Layout Extraction
4. Fully appreciate the design and analyze of CMOS Digital Circuits
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

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M.Tech. I Sem.

L	T	P	C
2	0	0	2

(25D57107) RESEARCH METHODOLOGY AND IPR

Course Category	Mandatory Course (credit)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the research design process and data collection methods.
2. To develop skills in data analysis and reporting.
3. To familiarize students with intellectual property rights (IPR) and patents.
4. To apply research skills in real-world contexts.

UNIT-I FUNDAMENTALS OF RESEARCH METHODOLOGY

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

Learning Outcomes

- Recall key concepts of the research process, including different types and approaches to research, and the importance of ethics.
 - Differentiate between qualitative and quantitative research approaches and the various uses of secondary data.
 - Identify the core principles of research design and ethics, including plagiarism and documentation styles.
 - Explain the significance of reasoning and ethical conduct in all stages of the research process.
- Apply knowledge of different documentation styles, such as APA and IEEE, to properly cite sources and avoid plagiarism.

UNIT-II DATA COLLECTION AND SOURCES

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

Learning Outcomes

- Identify different types of data and the various methods for collecting both primary and secondary data.
 - Explain the importance of data quality and ethical considerations in data collection.
 - Differentiate between primary, secondary, and Big Data sources.
 - Describe the various tools and technologies used for effective data collection.
- Analyze the ethical implications of data collection and ensure data quality in a research study.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-III DATA ANALYSIS AND REPORTING

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

Learning Outcomes

- Apply knowledge of multivariate analysis and experimental research to develop hypotheses and analyze data.
- Explain the process of measurement systems analysis and error propagation in experimental design.
- Formulate clear and concise abstracts, introductions, and methodologies for research papers.
- Write effective results and discussion sections based on data analysis.
Develop comprehensive research papers and proposals based on proper data analysis and reporting guidelines.

UNIT-IV UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Learning Outcomes

- Recall the fundamental concepts of Intellectual Property (IP) and its evolution.
- Describe the roles of organizations like **WIPO** and **WTO** in the establishment of IPR.
- Differentiate between various types of IPR, including trade secrets and trademarks.
- Explain the common rules and features of IPR agreements and the role of UNESCO.
Analyze the relationship between IPR and biodiversity, and its broader impact.

UNIT-V PATENTS

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Learning Outcomes

- Explain the objectives, benefits, and key features of a patent, including the concept of an inventive step.
- Differentiate between the various types of patent applications and the e-filing process.
- Describe the process of patent examination, grant, and revocation.
- Identify the roles of patent agents and the process for their registration.
Analyze the concepts of equitable assignments, licenses, and licensing of related patents.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004
2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.



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REFERENCE BOOKS:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners. David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.
6. Peter Elbow, Writing with Power, Oxford University Press, 1998.

e-Resources and Digital Material:

1. Coursera / edX – Research Methodology and Data Analysis courses
2. Springer Link & ScienceDirect – Latest journals on research design and statistics
3. Google Scholar – Free access to research papers
4. NCBI Bookshelf – Open-access research methodology resources
5. Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

COURSE OUTCOMES:

1. Recall key concepts and terminology related to research design, data collection, and intellectual property rights.
2. Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.
3. Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.
4. Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.
5. Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods. 6. Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
0	1	2	2

(25D57108) RTL SYNTHESIS, SIMULATION AND VERIFICATION

Course Category	Skill Oriented Course (SC)
Course Enrichment Relevance	Skill Development

COURSE OBJECTIVES:

1. The simulation of combinational and sequential circuits.
2. FSM based designs.
3. Implementation of DFT and FFTs.
4. Verify layout of basic digital circuits.

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (System Verilog/VHDL basics).
- Lab:
 1. Write synthesizable Verilog/System Verilog code for:
 - a) Half Adder, Full Adder
 - b) 4-bit Ripple Carry Adder
 - c) 4-bit Synchronous Counter (Up/Down)
 2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:
 1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
 2. Generate gate-level netlist and analyze area, delay, power reports.
 3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations
 1. Develop testbenches for:
 - a) 4-bit ALU (add, sub, AND, OR).
 - b) Universal Shift Register.
 2. Perform functional simulation using EDA tools
 3. Perform post-synthesis (timing) simulation and compare results with functional simulation.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.
 1. Write self-checking testbenches for combinational and sequential circuits.
 2. Use assertion-based verification (System Verilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
 3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:
 1. UART Transmitter/Receiver
 2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
 3. FIFO Buffer with full/empty flags

TEXT BOOKS:

1. Samir Palanitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson, 2007.
2. Michael Ciletti – Advanced Digital Design with the Verilog HDL.
3. Chris Spear & Greg Tumbush – System Verilog for Verification.
4. David Rich – Design and Verification with System Verilog.
5. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall 2003.
6. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx, 2011.

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs.
5. Build and verify various digital circuits.4. Employ simulation and formal verification methodologies, including assertion-based verification and equivalence checking.
6. Integrate RTL modules and perform case-study designs covering hierarchical design, DFT, HLS, and FPGA implementation.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109A) ENGLISH FOR RESEARCH PAPER WRITING (AC-I)

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To equip students with the fundamentals of academic English for research paper writing.
2. To develop students' advanced reading skills for analyzing and evaluating research articles.
3. To refine students' grammar and language skills for clarity and precision in research writing.
4. To master the skills of revising, editing, and proofreading research papers.
5. To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.

UNIT-I FUNDAMENTALS OF ACADEMIC ENGLISH

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills - Framing Title and Sub-headings

UNIT-II READING SKILLS FOR RESEARCHERS

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT-III GRAMMAR REFINEMENT FOR RESEARCH WRITING

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT-IV MASTERY IN REFINING WRITTEN CONTENT/EDITING SKILLS

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision - Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

UNIT-V TECHNOLOGY AND LANGUAGE FOR RESEARCH

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing - Assistance in Generating Citations and References - Plagiarism and Ethical Considerations - Tools and Awareness - Fair Practices



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge, 2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

REFERENCE BOOKS:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing with Power, E-book, Oxford University Press, 2007
3. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005
4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R. Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R. How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

e-Resources and Digital Material:

1. <https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/>
2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview
3. Writing in the Sciences" – Stanford University (MOOC on Coursera) <https://www.coursera.org/learn/sciwrite>
4. Academic Phrasebank – University of Manchester <http://www.phrasebank.manchester.ac.uk>
5. OWL (Online Writing Lab) – Purdue University, <https://owl.purdue.edu> *(Resources on APA/MLA formats, grammar, structure, paraphrasing) *
6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources

COURSE OUTCOMES:

1. Recall the key language aspects and structural elements of academic writing in research papers.
2. Explain the importance of clarity, precision, and objectivity in research writing.
3. Apply critical reading strategies and advanced grammar skills to analyze and write research papers.
4. Analyze research articles and identify the strengths and limitations of different methodologies.
5. Evaluate research papers to check for plagiarism, structure, clarity, and language accuracy.
6. Evaluate the effectiveness of different language and technology tools in research writing, including AI-assisted tools and plagiarism detection software and Develop a well-structured research paper that effectively communicates complex ideas.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109B) VALUE EDUCATION (AC-I)

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Human Values

COURSE OBJECTIVES:**UNIT-I VALUES AND SELF-DEVELOPMENT**

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II IMPORTANCE OF VALUES

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III PERSONALITY AND BEHAVIOR DEVELOPMENT

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV AVOID FAULT THINKING

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V CHARACTER AND COMPETENCE

Character and Competence –Holy books vs Blind faith. Self-management and good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

COURSE OUTCOMES:

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109C) DISASTER MANAGEMENT (AC-I)

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Environment & Sustainability

COURSE OBJECTIVES:

1. To enable the students to understand the fundamental concepts of disasters, hazards, their factors, and significance with special reference to India.
2. To prepare them to classify and analyze different types of natural and man-made disasters, their causes, magnitude, and impacts.
3. To foster them develop understanding of disaster preparedness, monitoring systems, and the role of government, community, and media.
4. To equip them in learning risk assessment techniques, disaster risk reduction strategies, and the importance of global and national cooperation.
5. To foster their ability to think critically and respond to disasters and design effective mitigation measures (structural and non-structural) with a focus on emerging trends and Indian disaster management programs.

UNIT-I INTRODUCTION & DISASTER PRONE AREAS IN INDIA

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT-II REPERCUSSIONS OF DISASTERS AND HAZARDS

Economic Damage - Loss of Human and Animal Life - Destruction of Ecosystem - Natural Disasters - Earthquakes, Volcanism, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster - Nuclear Reactor Meltdown - Industrial Accidents - Oil Slick and Spills - Outbreaks of Disease and Epidemics War and Conflicts

UNIT-III DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness - Monitoring of Phenomena - Triggering a Disaster or Hazard - Evaluation of Risk - Application of Remote Sensing - Data from Meteorological and Other Agencies - Media Reports - Governmental and Community Preparedness

UNIT-IV RISK ASSESSMENT DISASTER RISK

Disaster Risk - Concept and Elements, Disaster Risk Reduction - Global and National Disaster Risk Situation - Techniques of Risk Assessment - Global Co-Operation in Risk Assessment and Warning - People's participation in Risk Assessment - Strategies for Survival

UNIT-V DISASTER MITIGATION

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Gupta, H. K. Disaster Management. Universities Press, 2003
2. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.

REFERENCE BOOKS:

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.
4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.
5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

e-Resources and Digital Material:

1. National Disaster Management Authority (NDMA), India: <https://ndma.gov.in> – official guidelines, reports, and policy frameworks.
2. United Nations Office for Disaster Risk Reduction (UNDRR): <https://www.undrr.org> – Sendai Framework, global risk reduction strategies.
3. Global Disaster Alert and Coordination System (GDACS): <https://www.gdacs.org> – real-time disaster alerts.
4. World Health Organization (WHO) – <https://www.who.int/emergencies> – disaster-related health guidelines.

COURSE OUTCOMES:

1. Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.
2. Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters.
3. Assess the economic, social, and ecological repercussions of major natural and man-made disasters.
4. Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.
5. Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.
6. Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. I Sem.

L	T	P	C
2	0	0	0

**(25D57109D) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE
(AC-I)**

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Human Values

COURSE OBJECTIVES:

1. To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.
2. To make them understand the need for protecting traditional knowledge and its significance in the global economy.
3. To make them understand the legal frame work and policies related to traditional knowledge protection.
4. To enable them to understand the relationship between traditional knowledge and intellectual property rights.
5. To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

UNIT-I INTRODUCTION TO TRADITIONAL KNOWLEDGE

Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) - Characteristics - traditional knowledge vis-à-vis indigenous knowledge - Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge.

UNIT-II PROTECTION, NEED, SIGNIFICANCE, VALUE AND ROLE OF TRADITIONAL KNOWLEDGE

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK

UNIT-III LEGAL FRAME WORK

Legal frame work and TK - A) The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) - B) The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

UNIT-IV TRADITIONAL KNOWLEDGE AND INTELLECTUAL PROPERTY

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.



SANTHIRAM ENGINEERING COLLEGE

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UNIT-V TRADITIONAL KNOWLEDGE IN DIFFERENT SECTORS

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

TEXT BOOKS:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt. Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh, Traditional Knowledge System and Technology in India, Pratibha Prakashan 2012.

REFERENCE BOOKS:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh, Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

e-Resources and Digital Material:

1. <https://www.youtube.com/watch?v=LZP1StpYEPm>
2. <http://nptel.ac.in/courses/121106003/>

COURSE OUTCOMES:

1. Define and explain the concept of traditional knowledge, its nature, characteristics, and scope
2. Understand the need for protecting traditional knowledge and its significance in the global economy
3. Explain the legal framework and policies related to traditional knowledge protection
4. Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology
5. Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change
6. Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms



**M. Tech (VLSISD Branch)
II-Semester
Course Structure**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN****M.Tech. II Sem. - Course Structure**

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				L	T	P	C	IM	EM	Total
1	25D57201	PC	CMOS MIXED SIGNAL IC DESIGN	3	0	0	3	40	60	100
2	25D57202	PC	PHYSICAL DESIGN AUTOMATION	3	0	0	3	40	60	100
3	25D57203A	PE	DIGITAL VLSI TESTING (PE-III)	3	0	0	3	40	60	100
4	25D57203B	PE	INTEGRATED CIRCUITS, MOSFETS, OP-AMPS AND THEIR APPLICATIONS (PE-III)	3	0	0	3	40	60	100
5	25D57203C	PE	SOC TESTING AND VERIFICATION (PE-III)	3	0	0	3	40	60	100
6	25D57203D	PE	SEMICONDUCTOR MEMORY DESIGN AND TESTING (PE-III)	3	0	0	3	40	60	100
7	25D57203E	PE	ADVANCED VLSI INTERCONNECTS (PE-III)	3	0	0	3	40	60	100
8	25D57204A	PE	SEMICONDUCTOR DEVICES FOR NEXT GENERATION FETS: A PHYSICS PERSPECTIVE (PE-IV)	3	0	0	3	40	60	100
9	25D57204B	PE	DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS (PE-IV)	3	0	0	3	40	60	100
10	25D57204C	PE	ALGORITHMS FOR VLSI DESIGN (PE-IV)	3	0	0	3	40	60	100
11	25D57204D	PE	LOW POWER VLSI DESIGN (PE-IV)	3	0	0	2	40	60	100
12	25D57204E	PE	VLSI SIGNAL PROCESSING (PE-IV)	3	0	0	2	40	60	100
13	25D57205	PC	CMOS MIXED SIGNAL IC DESIGN LAB	0	0	4	2	40	60	100
14	25D57206	PC	PHYSICAL DESIGN AUTOMATION LAB	0	0	4	2	40	60	100
15	25D57207	MC(C)	QUANTUM TECHNOLOGIES AND APPLICATIONS	2	0	0	2	40	60	100
16	25D57209A	PE	ENTREPRENEURSHIP ESSENTIALS (AC-II)	2	0	0	0	40	0	40
17	25D57209B	PE	PEDAGOGY STUDIES (AC-II)	2	0	0	0	40	0	40
18	25D57209C	PE	YOGA FOR STRESS MANAGEMENT(AC-II)	2	0	0	0	40	0	40
19	25D57209D	MC(NC)	CONSTITUTION OF INDIA (AC-II)	2	0	0	0	40	0	40
20	25D57208	PR	COMPREHENSIVE VIVA VOCE	0	0	0	2	0	100	100



**M. Tech (VLSISD Branch)
II-Semester
Syllabus**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57201) CMOS MIXED SIGNAL IC DESIGN

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To demonstrate first order filter with least interference
2. To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects
3. To design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I SWITCHED CAPACITOR CIRCUITS

: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT-II PHASED LOCK LOOP (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III DATA CONVERTER

Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV A TO D CONVERTERS

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D converters, Time- interleaved converters

UNIT-V OVERSAMPLING CONVERTERS

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010
2. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009

COURSE OUTCOMES:

1. To understand, analyze and design Switched capacitor filter circuits
2. To analyze and design the PLL circuits
3. To analyze and design the different D/A converters
4. To analyze and design the different A/D converters
5. To analyze modulators, filters and converters.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57202) PHYSICAL DESIGN AUTOMATION

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand relation between automation algorithms and constraints posed by VLSI technology
2. To adopt algorithms to meet critical design parameters.
3. To design area efficient logics by employing different routing algorithms and shape functions
4. To simulate and synthesis different combinational and sequential logics

UNIT-I VLSI DESIGN AUTOMATION TOOLS

Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT-II LAYOUT

Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT-III FLOOR PLANNING AND ROUTING

Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT-IV SIMULATION AND LOGIC SYNTHESIS

Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis

UNIT-V HIGH-LEVEL SYNTHESIS

Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999

REFERENCE BOOKS:

1. S.M. Sait, H. Youssef, VLSI Physical Design Automation, World scientific, 1999
2. M. Sarraf Zadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. To understand the various VLSI design flows and applications in the VLSI technology
2. To remember the design rules and apply in the VLSI design verification process.
3. To understand and apply routing and placement algorithms to meet critical design parameters
4. To evaluate the VLSI design for logical synthesis using simulation tools
5. To apply various synthesis models for the different combinational and sequential circuits.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203A) DIGITAL VLSI TESTING (PE-III)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To introduce the importance of testing in the VLSI design cycle and the challenges associated with modern complex IC designs
2. To explain the fault models, test generation methods, and fault simulation techniques essential for detecting and diagnosing design defects
3. To familiarize students with the principles and architectures of Design for Testability (DFT) for efficient test implementation
4. To develop understanding of built-in self-test (BIST), scan design, and boundary scan architectures for improved test coverage and yield
5. To enable learners to design VLSI systems with testability features ensuring reliability, manufacturability, and cost-effectiveness

UNIT-I FUNDAMENTALS OF VLSI TESTING

Introduction: Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues

UNIT-II DESIGN FOR TESTABILITY (DFT) TECHNIQUES

Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture, Scan design rules, Scan design flow. Fault Simulation: Introduction, Simulation models

UNIT-III FAULT SIMULATION AND TEST GENERATION

Fault Simulation: Logic simulation, Fault simulation. Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms. ATPG for non-stuck-at faults, other issues in test generation Built-In-Self-Test: Introduction, BIST design rules

UNIT-IV BUILT-IN-SELF-TEST (BIST) AND TEST COMPRESSION

Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures. Test Compression: Introduction, Stimulus compression, Response compression.

UNIT-V MEMORY, POWER, AND THERMAL AWARE TESTING

Memory Testing: Introduction, RAM fault models, RAM test generation. Memory Testing: Memory BIST Power and Thermal Aware Test: Importance, Power models, Low power ATPG. Power and Thermal Aware Test: Low power BIST, Thermal aware techniques



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2000
2. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann Publishers, 2006
3. N. K. Jha and S. Gupta, Testing of Digital Systems, Cambridge University Press, 2003.
4. P. K. Lala, Digital Circuit Testing and Testability, Academic Press, 1997
5. B. K. Singh, VLSI Testing and Design for Testability, New Age International Publishers, 2020

REFERENCE BOOKS:

1. Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1994.
2. Charles E. Stroud, A Designer's Guide to Built-In Self-Test, Springer, 2002.

COURSE OUTCOMES:

1. Explain the role and significance of testing in the VLSI design process and its impact on product yield and quality.
2. Identify and analyze various fault models and apply test generation algorithms to detect faults in digital circuits.
3. Design circuits incorporating DFT techniques such as scan chains, boundary scan, and BIST architectures.
4. Evaluate the effectiveness of different testing strategies in achieving high fault coverage and manufacturability.
5. Apply VLSI testing principles and DFT methodologies to design reliable and testable integrated circuits for large-scale production

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

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3	0	0	3

(25D57203B) INTEGRATED CIRCUITS, MOSFETS, OP-AMPS AND THEIR APPLICATIONS (PE-III)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To provide fundamental knowledge of IC fabrication processes, MOSFET parameters, and Op-Amp characteristics
2. To enable students to understand the principles of operational amplifiers and their internal circuit architecture
3. To familiarize students with various feedback techniques and types of noise encountered in analog circuits.
4. To develop the ability to design and analyze amplifiers, oscillators, and filters using operational amplifiers
5. To cultivate practical skills in constructing, testing, and troubleshooting analog electronic circuits

UNIT-I FUNDAMENTALS OF INTEGRATED CIRCUIT TECHNOLOGY

Introduction to Integrated Circuit (IC) Technology, Evolution and Importance of ICs, Fabrication Processes for Integrated Circuits, Basic IC Manufacturing Steps: Oxidation, Diffusion, Ion Implantation, Photolithography, Metallization, Overview of Bipolar and MOS Technologies.

UNIT-II OPERATIONAL AMPLIFIERS

Fundamentals and Characteristics:

Introduction to Operational Amplifiers (Op-Amps), Characteristics and Internal Structure of Op-Amps, Common Mode Rejection Ratio (CMRR) and its Importance, Input Offset Voltages, Input Bias, and Offset Currents, Frequency Response of Op-Amps.

UNIT-III MOSFET TECHNOLOGY AND APPLICATIONS

MOSFET Fabrication Techniques and Structure, MOSFET Characteristics and Applications, Current Mirrors using MOSFETs, Design and Analysis of Current Mirror Circuits in Integrated Systems.

UNIT-IV FEEDBACK, AMPLIFIERS, AND SIGNAL PROCESSING CIRCUITS

Frequency Response and Feedback Techniques in ICs, Design and Analysis of Comparators and Instrumentation Amplifiers, Active Filters and their Realizations, Oscillator Design using Op-Amps and MOS Circuits.

UNIT-V DATA CONVERSION AND PRACTICAL OP-AMP APPLICATIONS

Noise in Electronic Circuits, Op-Amp Based Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC) using Op-Amps, Reading and Interpreting Op-Amp Datasheets, Design Considerations and Real-World Applications



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition
2. CMOS Digital Integrated Circuits Analysis and Design Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011

REFERENCE BOOKS:

1. Gray, Hurst, Lewis, and Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, 5th edition, 2009
2. Horowitz and Hill, The Art of Electronics, Cambridge Univ. Press, 1999
3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001

COURSE OUTCOMES:

1. Understand and analyze the characteristics and operation of operational amplifiers.
2. Demonstrate knowledge of IC fabrication technology and the equipment used in integrated circuit manufacturing.
3. Explain different feedback configurations and identify sources and effects of noise in analog systems
4. Design and analyze various amplifier and oscillator circuits using operational amplifiers.
5. Design, simulate, and troubleshoot analog filters and other practical analog circuits using Op-Amps.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203C) SOC TESTING AND VERIFICATION (PE-III)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the concepts of faults and testing in SoC
2. To implement the faults using simulation tools
3. To analyze BIST systems

UNIT-I INTRODUCTION TO TESTING

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II LOGIC AND FAULT SIMULATION

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT-III TESTABILITY MEASURES

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV BUILT-IN SELF-TEST

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V

Boundary Scan Standard:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BSDL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers
2. M. Abramovici, M.A. Breuer and A.D Friedman, Digital Systems and Testable Design, Jaico Publishing House.

REFERENCE BOOKS:

1. P.K. Lala, Digital Circuits Testing and Testability, Academic Press

COURSE OUTCOMES:

1. To understand the types faults and the concepts of faults and testing in SoC
2. To understand the algorithms to detect the faults using simulation tools.
3. To understand and apply the concepts of observability and controllability.
4. To apply and evaluate the circuit under test using BIST
5. To apply and evaluate the circuit under test using Boundary Scan tests.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

**(25D57203D) SEMICONDUCTOR MEMORY DESIGN AND TESTING
(PE-III)**

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand different types of memories, their architectural and different packing techniques of memories.
2. To build fault models for memory testing
3. To analyze different parameters that lead malfunctioning of memories
4. To design reliable memories with efficient architecture to improve processes times and power.

UNIT-I RANDOM ACCESS MEMORY TECHNOLOGIES

SRAM: SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II NON-VOLATILE MEMORIES

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One-time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT-III MEMORY FAULT MODELING TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT-V ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKING TECHNOLOGIES

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.



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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Semiconductor Memories Technology Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley

REFERENCE BOOKS:

1. Modern Semiconductor Devices for Integrated Circuits Chenming C Hu, First Edition. Prentice all

COURSE OUTCOMES:

1. To understand and analyze the SRAM and DRAM cell structures
2. To understand, remember and apply different types of memory cells in suitable applications
3. To analyze and evaluate fault models for memory testing
4. To analyze the memories for reliability and radiation effects
5. To understand and remember advanced manufacturing technologies in memory cell designs.

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M.Tech. II Sem.

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3	0	0	3

(25D57203E) ADVANCED VLSI INTERCONNECTS (PE-III)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the fundamentals of VLSI interconnect modeling and delay estimation.
2. To study distributed RC and RLC interconnect models and analyze signal propagation delays.
3. To explore inductive, skin, and electromigration effects influencing interconnect performance.
4. To analyze and mitigate crosstalk and extract key interconnect parameters.
5. To introduce quantum effects in nanoscale and graphene-based interconnects.

UNIT-I INTRODUCTION TO VLSI INTERCONNECTS

Introduction to VLSI Interconnects, the Distributed RC Interconnect Model, Elmore Delay in Interconnects, and Scaling Effects in Interconnects. Simulation and Delay Mitigation Techniques in RC Interconnects

UNIT-II INDUCTIVE EFFECTS IN INTERCONNECTS

Inductive Effects in Interconnects, Distributed RLC Interconnect Model, and Transmission Line Equations. When to Consider Inductive Effects, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, and RLC Interconnect Simulation Techniques.

UNIT-III SKIN EFFECT AND ELECTROMIGRATION

Origin of the Skin Effect and its Impact on Signal Integrity, Effective Resistance at High Frequencies, and Power Dissipation in Interconnects. Electromigration in Interconnects, Physical Mechanisms, Reliability Issues, and Mitigation Techniques for Electromigration.

UNIT-IV CROSSTALK AND PARAMETER EXTRACTION

Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, and Crosstalk Mitigation Techniques. Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance and Inductance, Estimation of Interconnect Parameters from S-Parameters

UNIT-V QUANTUM EFFECTS IN INTERCONNECTS

Quantum Conductance and Quantum Capacitance, Kinetic Inductance, and Graphene Nanoribbon Interconnects. Quantum Effects in Nanoscale Interconnects, Analysis and Simulation of Interconnects Considering Quantum Effects.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Banerjee, K., and Mehrotra, A., Analysis and Optimization of On-Chip Inductive Interconnects, Springer, 2001
2. Bakoglu, H. B., Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, 1990.

REFERENCE BOOKS:

1. Deutsch, A., et al., High-Speed Signal Propagation: Advanced Black Magic, Prentice Hall, 2003.
2. Rabaey, J. M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall, 2003.
3. Zhang, L., and Joshi, R. V., Interconnect Analysis and Design for Advanced VLSI, Springer, 201

COURSE OUTCOMES:

1. Understand the distributed RC and RLC models for on-chip interconnects.
2. Analyze the delay and signal integrity issues caused by inductive and resistive effects.
3. Identify and mitigate electromigration and skin effect problems in interconnects.
4. Evaluate and simulate crosstalk and extract interconnect parameters effectively.
5. Apply quantum and nanoscale interconnect concepts in advanced VLSI systems

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M.Tech. II Sem.

L	T	P	C
3	0	0	3

**(25D57204A) SEMICONDUCTOR DEVICES FOR NEXT GENERATION
FETS: A PHYSICS PERSPECTIVE (PE-IV)**

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To introduce the fundamental principles of Metal-Oxide-Semiconductor (MOS) capacitors and their role in the operation of MOS-based devices
2. To provide a comprehensive understanding of various Field-Effect Transistor (FET) architectures, including MOSFETs, FinFETs, GAA FETs, and High-Power FETs
3. To explore the challenges, limitations, and scaling issues in conventional CMOS technology and motivate the need for beyond-CMOS devices
4. To familiarize students with emerging device technologies such as Negative Capacitance FETs (NC-FETs) and 2D material-based transistors for future nano electronic applications
5. To enable learners to analyze device performance parameters and understand their implications for modern VLSI circuit design and fabrication

UNIT-I MOS CAPACITORS AND MOSFET FUNDAMENTALS

MOS Capacitors: Introduction of Metal-Oxide-Semiconductor, Energy Band Diagram of MOS Capacitors, Second Order Effects in MOS Capacitors, C-V of MOS capacitor

MOSFET and Application: Introduction of MOSFET, I-V and C-V Characteristics of MOSFETs, Capacitance Modeling for HF & LF, High and Low Frequency Modeling in Bulk MOSFET, MOSFET as Switch and Amplifier

MOSFET SPICE Models: Introduction to MOSFET SPICE Models, Discuss Various SPICE Models equations, SPICE Models for the MOS Transistor, The SPICE Diode Models, Practical Aspects and Simulation Techniques

UNIT-II ADVANCED MOSFET ARCHITECTURES AND SHORT-CHANNEL EFFECTS

Semiconductor Heterostructures: Introduction, Carriers and Transports, Band Diagram of Heterostructure, PN Heterojunction Diode, Properties and Application

Short Channel Effects: Introduction to 2nd Order Effects at Lower Technology Node, Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), and Subthreshold Swing (SS), Mobility and Scattering Effects, Velocity Saturation Effects, Hot Carrier Effect, Self-heating Effect

Double Gate MOSFET: Introduction to Double Gate MOSFET, SOI MOSFET, Partially and Fully Depleted MOSFET, Subthreshold Swing and Transconductance, Small and Large Signal Modeling, Introduction of Junction less MOSFET

UNIT-III EMERGING TRANSISTOR TECHNOLOGIES

FinFET and GAA FET:

FinFET: A successor of MOSFET, Introduction to FinFETs Structure, Structural Classification of FinFETs, RLC FinFET Modeling, High Frequency Small Signal Modeling, Device Circuit Co-Design using FinFET with Suitable Examples

Gate-All-Around FETs: Sub 5nm Node Devices: Introduction of Different Types of GAA Structure, Current Trends in GAA Devices, Nanosheet FET, Process Variation in



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

Nanosheet FET, Analog Perspective of Nanosheet FET

Forksheet FET and CFET: Sub 3nm Node, Introduction to Forksheet FET, Discuss the challenges of Forksheet, CFET Advancements and Industry Adoption, Discuss the Circuit Design Challenges with CFET, CFET Optimization for Semiconductor Scaling

UNIT-IV BEYOND-CMOS DEVICES AND NOVEL CONCEPTS

Negative Capacitance: Improved Subthreshold Swing: Negative Capacitance (NC): A Concept Note, FeFET & FeFET Based Memory, Advantages and Challenges of NCFETs, Modelling of NCFETs, Introduction of Phase Transition Material (PTM). III-V Semiconductor FETs: Introduction of III-V materials, Materials for High-Speed Devices and Circuits, High Electron Mobility Transistors (HEMT): Modelling and Simulation, III-V Semiconductor FET, Application of III-V material-based FET.

UNIT-V 2D MATERIAL-BASED DEVICES AND FUTURE NANOELECTRONICS

2D Materials for Next Generation Computing: Fundamental Understanding of 2D Material, Physics Properties of 2D Materials, Challenges and Future Scope, Application of 2D Material, 2D-FETs

TEXT BOOKS:

1. Neamen, Donald A. Semiconductor physics and devices: basic principles. New York, NY: McGraw-Hill, 2012.
2. R. F. Pierret, Semiconductor Device Fundamentals, 1996.
3. Jean-Pierre Colinge, FinFETs and Other Multi-Gate Transistors, 2008.

REFERENCE BOOKS:

1. S. M. Sze and M. K. Lee, Semiconductor Devices: Physics and Technology, 3rd Edition, Wiley, 2012.
2. D. Nirmal, J. Ajayan, and P. J. Fay (Editors), Semiconductor Devices and Technologies for Future Ultra Low Power Electronics, CRC Press, 2021.
3. S. Tayal, A. K. Sharma, and A. K. Singh (Editors), Advanced Ultra Low-Power Semiconductor Devices: Design and Applications, Scrivener Publishing, Wiley, 2022.

e-Resources and Digital Material:

1. https://onlinecourses.nptel.ac.in/noc25_ee75/preview

COURSE OUTCOMES:

1. Explain the structure and operation of MOS capacitors and the principles governing charge, capacitance, and threshold behavior
2. Analyze and compare different types of FETs based on their device structures, electrical characteristics, and fabrication techniques
3. Evaluate the technological limitations of CMOS scaling and identify potential solutions through novel device architectures
4. Demonstrate an understanding of next-generation transistor technologies such as NC-FETs, GAA-FETs, and 2D-material-based devices in the context of VLSI evolution.
5. Apply the acquired knowledge to assess device suitability for low-power, high-performance, and high-density VLSI design applications.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

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3	0	0	3

(25D57204B) DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS (PE-IV)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I CMOS DEVICE FUNDAMENTALS AND INVERTER CHARACTERISTICS**

CMOS transistor fundamentals and current modeling, CMOS inverter structure and voltage transfer characteristics, Noise margins and switching thresholds, Dynamic behavior and delay modeling of CMOS inverters.

UNIT-II DELAY ANALYSIS AND OPTIMIZATION IN CMOS CIRCUITS

RC delay modeling in interconnects and logic paths, Delay estimation using logical effort and Elmore delay, Techniques for delay and performance optimization, Trade-offs among delay, area, and power metrics

UNIT-III LOGIC DESIGN STYLES AND INTERCONNECT MODELING

Overview of CMOS combinational circuit families (static, dynamic, pass-transistor logic), Stick diagrams and layout representations, Interconnect modeling: resistance, capacitance, and delay considerations, Interconnect scaling, signal integrity, and crosstalk effects.

UNIT-IV POWER OPTIMIZATION AND SEQUENTIAL DESIGN

Power dissipation components in CMOS circuits: dynamic, static, and short-circuit power, Power estimation and reduction techniques, Design and analysis of CMOS latches and flip-flops, Timing parameters: setup time, hold time, clock skew, and static timing analysis.

UNIT-V DATAPATH AND APPROXIMATE COMPUTING SUBSYSTEM

Design of arithmetic subsystems: adders and related datapath elements, Approximate computing concepts and design trade-offs, Error metrics and performance evaluation in approximate subsystems, Case studies on power-performance-accuracy optimization.

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikoli, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2016.
2. Neil H.E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, 2015.
3. S.M. Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, McGraw-Hill Education, 2019.

REFERENCE BOOKS:

1. Kiat-Seng Yeo & Kaushik Roy, Low-Voltage, Low-Power VLSI Subsystems, McGraw-Hill Professional, 2004.
2. Kaushik Roy & Sharat C. Prasad, Low-Power CMOS VLSI Circuit Design, John Wiley & Sons, 2000.
3. Ajit Pal, Low-Power VLSI Circuits and Systems, Springer India, 2015.
4. Ming-Bo Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective, CRC Press, 2012.



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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Introduce the fundamental design metrics-delay, power, and area-in Digital CMOS VLSI subsystem design.
2. Develop the ability to estimate and optimize power consumption in CMOS logic circuits and interconnects.
3. Analyze interconnect-aware design challenges and explore strategies for delay and energy optimization in subsystems
4. Familiarize students with approximate computing concepts, datapath subsystem design, and associated error metrics.
5. Explain the design principles, timing parameters, and trade-offs involved in sequential circuit elements such as latches and flip-flops.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57204C) ALGORITHMS FOR VLSI DESIGN (PE-IV)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To impart knowledge about the computer arithmetic algorithms, including different techniques enabling enhanced throughput and low power.
2. To understand algorithms techniques to hardware implementation of various arithmetic operations.

UNIT-I NUMBERS AND ARITHMETIC

Review of Number Systems, Their Encoding, and Basic Arithmetic Operations. Class of Fixed-Radix Number Systems and Unconventional Fixed-Point Number Systems. Representing Signed Numbers, Negative-Radix Number Systems, Redundant Number Systems, and Residue Number Systems.

UNIT-II ALGORITHMS FOR FAST ADDITION

Basic Addition and Counting, Bit-Serial and Ripple-Carry Adders, Addition of a Constant (Counters), Manchester Carry Chains and Adders, Carry-Look-Ahead Adders, Carry Determination as Prefix Computation, and Alternative Parallel Prefix Networks. VLSI Implementation Aspects, Variations in Fast Adders, Simple Carry-Skip and Carry-Select Adders, Hybrid Adder Designs, and Optimizations in Fast Adders. Multi-Operand Addition, Wallace and Dadda Trees, Parallel Counters, Generalized Parallel Counters, and Adding Multiple Signed Numbers.

UNIT-III HIGH-SPEED MULTIPLICATION

Basic Multiplication Schemes, Shift/Add Multiplication Algorithms, Programmed Multiplication, and Basic Hardware Multipliers. Multiplication of Signed Numbers and Multiplication by Constants. Overview of Fast Multipliers, High-Radix Multipliers, Modified Booth's Recoding, Tree and Array Multipliers, Variations in Multipliers, and VLSI Layout Considerations.

UNIT-IV FAST DIVISION AND DIVISION THROUGH MULTIPLICATION

Basic Division Schemes, Shift/Subtract Division Algorithms, Programmed Division, Restoring and Non-Restoring Hardware Dividers, and Signed Division. Division by Constants, Fast Divider Techniques, High-Radix Dividers, Variations in Dividers, Combined Multiply/Divide Units, Division by Convergence, and Hardware Implementation Approaches.

UNIT-V REAL ARITHMETIC AND IMPLEMENTATION TOPICS

Representing Real Numbers, Floating-Point Arithmetic, ANSI/IEEE Floating-Point Standard, Exceptions and Features, Floating-Point Arithmetic Operations, and Rounding Schemes. Logarithmic Number Systems, Floating-Point Adders, Barrel-Shifter Design, Leading-Zeros/Ones Counting, Floating-Point Multipliers and Dividers. Arithmetic Errors and Error Control, Computing Algorithms, Exponentiation, Approximating Functions, Merged Arithmetic, Arithmetic by Table Lookup, Trade-offs in Cost, Speed, and Accuracy, High-Throughput Arithmetic, Low-Power Arithmetic, Fault-Tolerant Arithmetic, Emerging Trends, and Impact of Hardware Technology.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Computer Arithmetic: Algorithms and Hardware Design by Parhami, B., Oxford University Press
2. Computer Arithmetic Algorithms by Koren, I., CRC Press

REFERENCE BOOKS:

1. Digital Arithmetic by Ercegovic, M. and Lang, T., Elsevier.
2. Verilog Digital Computer Design Algorithms into Hardware by Mark Gordon Arnold, Prentice Hall PTR. Zhang, L., and Joshi, R. V., Interconnect Analysis and Design for Advanced VLSI, Springer, 201

COURSE OUTCOMES:

1. Understand hardware implementation of various algorithms.
2. Learn to apply tradeoffs and multiple implementations and architectures.
3. Know the use cases of various algorithms and their considerations

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	2

(25D57204D) LOW POWER VLSI DESIGN (PE-IV)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. To implement Low power design approaches for system level and circuit level measures.
3. To design low power adders, multipliers and memories for efficient design of systems.

UNIT-I FUNDAMENTALS

Need for Low Power Circuit Design, Sources of Power Dissipation Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II LOW-POWER DESIGN APPROACHES

Low-Power Design through Voltage Scaling VTCMOS circuits, MTCMOS circuits, Architectural Level Approach Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III LOW-VOLTAGE LOW-POWER ADDERS

Introduction, Standard Adder Cells, CMOS Adders Architectures. Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques. Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles

UNIT-IV LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits Analysis and Design Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect.
2. Design Low power design approaches for system level and circuit level measures.
3. Design and evaluate low power adders for efficient design of systems.
4. Design and evaluate low power multipliers for efficient design of systems.
5. Design and evaluate low power memories for efficient design of systems.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
3	0	0	2

(25D57204E) VLSI SIGNAL PROCESSING (PE-IV)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To study the existing architectures suitable for VLSI
2. To understand the concepts of folding and unfolding algorithms and applications
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms

UNIT-I INTRODUCTION TO DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT-II FOLDING AND UNFOLDING

Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT-III SYSTOLIC ARCHITECTURE DESIGN

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT-IV FAST CONVOLUTION

Introduction Cook - Toom Algorithm Winograd algorithm Iterated Convolution Cyclic Convolution Design of Fast Convolution algorithm by Inspection.

UNIT-V LOW POWER DESIGN

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipelines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

TEXT BOOKS:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998
2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, Prentice Hall, 1985



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Jose E. France, Yannis Tsividis, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing, Prentice Hall, 1994
2. Medisetti V. K. VLSI Digital Signal Processing, IEEE Press (NY), 1995

COURSE OUTCOMES:

1. To study the existing architectures suitable for VLSI.
2. To understand the concepts of folding and unfolding algorithms and applications.
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms.
5. To apply low power approaches in the VLSI design for the signal processing.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(25D57205) CMOS MIXED SIGNAL IC DESIGN LAB

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To design and simulate op-amp for given specifications.
2. To design and simulate data converter for given specifications.
3. To design and simulate PLL and VCO for given specifications.
4. To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Cycle 1:

Fully compensated op-amp with resistor and miller compensation

High speed comparator design

Two stage cross coupled clamped comparator.

Strobed Flip-flop

Data converter

Cycle 2:

Switched capacitor circuits

Parasitic sensitive integrator

Parasitic insensitive integrator

Design of PLL

Design of VCO

Band gap reference circuit

Layouts of All the circuits Designed and Simulated

COURSE OUTCOMES:

1. Design and simulate op-amp for given specifications
2. Design and simulate data converter for given specifications
3. Design and simulate switched capacitor filters
4. Design and simulate PLL and VCO for given specifications
5. Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(25D57206) PHYSICAL DESIGN AUTOMATION LAB

Course Category	Professional Core course (PC)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To learn the implementation of different Physical Design Automation algorithms
2. To implement different graph algorithms
3. To implement different partitioning algorithms
4. To implement different floor planning algorithms
5. To implement different routing algorithms

Cycle 1:

Graph algorithms
Graph search algorithms
Depth first search
Breadth first search
Spanning tree algorithm
Kruskals algorithm
Shortest path algorithm
Dijkstra algorithm
Floyd- Warshall algorithm
Steiner tree algorithm
Computational geometry algorithm
Line sweep method
Extended line sweep method

Cycle 2:

Partitioning algorithms
Group migration algorithms
i) Kernighan Lin algorithm
Extensions of Kernighan-Lin algorithm
Fiduccias Mattheyses algorithm
Goldberg and Burstein algorithm
Simulated annealing and evolution algorithms
Simulated annealing algorithm
Simulated evolution algorithm
iii) Metric allocation method
Floor planning algorithms
Constraint based methods
Integer programming based methods
Rectangular dualization based methods
Hierarchical tree based methods
Simulated evolution algorithms
Time driven Floor planning algorithms



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

Routing algorithms

Two terminal algorithms

Maze routing algorithms

Lees algorithm

Soukups algorithm

Hadlock algorithm

Line-Probe algorithm

COURSE OUTCOMES:

1. Learn the implementation of different Physical Design Automation algorithms
2. Implement different graph algorithms
3. Implement different partitioning algorithms
4. Implement different floor planning algorithms
5. Implement different routing algorithms

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
2	0	0	2

(25D57207) QUANTUM TECHNOLOGIES AND APPLICATIONS

Course Category	Mandatory Course (credit)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Introduce fundamental quantum concepts like superposition and entanglement
2. Understand theoretical structure of qubits and quantum information
3. Explore conceptual challenges in building quantum computers.
4. Explain principles of quantum communication and computing
5. Examine real-world applications and the future of quantum technologies

UNIT-I INTRODUCTION TO QUANTUM THEORY AND TECHNOLOGIES

The transition from classical to quantum physics, Fundamental principles explained conceptually: Superposition, Entanglement, Uncertainty Principle, Wave-particle duality, Classical vs Quantum mechanics-theoretical comparison, Quantum states and measurement: nature of observation, Overview of quantum systems: electrons, photons, atoms, The concept of quantization: discrete energy levels, Why quantum Strategic, scientific, and technological significance, A snapshot of quantum technologies: Computing, Communication, and Sensing, National and global quantum missions: India's Quantum Mission, EU, USA, China.

UNIT-II THEORETICAL STRUCTURE OF QUANTUM INFORMATION SYSTEMS

What is a qubit Conceptual understanding using spin and polarization, Comparison: classical bits vs quantum bits, Quantum systems: trapped ions, superconducting circuits, photons (non-engineering view), Quantum coherence and decoherence intuitive explanation, Theoretical concepts: Hilbert spaces, quantum states, operators only interpreted in abstract, The role of entanglement and non-locality in systems, Quantum information vs classical information: principles and differences, Philosophical implications: randomness, determinism, and observer role.

UNIT-III BUILDING A QUANTUM COMPUTER THEORETICAL CHALLENGES AND REQUIREMENTS

is What a qubit Conceptual understanding using spin and polarization, Comparison: classical bits vs quantum bits, Quantum systems: trapped ions, superconducting circuits, photons (non-engineering view), Quantum coherence and decoherence intuitive explanation, Theoretical concepts: Hilbert spaces, quantum states, operators only interpreted in abstract, The role of entanglement and non-locality in systems, Quantum information vs classical information: principles and differences, Philosophical implications: randomness, determinism, and observer role.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV QUANTUM COMMUNICATION AND COMPUTING-THEORETICAL PERSPECTIVE

Quantum vs Classical Information, Basics of Quantum Communication, Quantum Key Distribution (QKD), Role of Entanglement in Communication, the Idea of the Quantum Internet Secure Global Networking, Introduction to Quantum Computing, Quantum Parallelism (Many States at Once), Classical vs Quantum Gates, Challenges: Decoherence and Error Correction, Real-World Importance and Future Potential.

UNIT-V APPLICATIONS, USE CASES AND THE QUANTUM FUTURE

Real-world application domains: Healthcare (drug discovery), Material science, Logistics and optimization, Quantum sensing and precision timing, Industrial case studies: IBM, Google, Microsoft, Quantum, Ethical, societal, and policy considerations, Challenges to adoption: cost, skills, standardization, Emerging careers in quantum: roles, skillsets, and preparation pathways, Educational and research landscape India's opportunity in the global quantum race.

TEXT BOOKS:

1. Michael A. Nielsen, Isaac L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 10th Anniversary Edition, 2010.
2. Eleanor Rieffel and Wolfgang Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011.
3. Chris Bernhardt, Quantum Computing for Everyone, MIT Press, 2019

REFERENCE BOOKS:

1. David McMahon, Quantum Computing Explained, Wiley, 2008
2. Phillip Kaye, Raymond Laflamme, Michele Mosca, An Introduction to Quantum Computing, Oxford University Press, 2007.
3. Scott Aaronson, Quantum Computing Since Democritus, Cambridge University Press, 2013
4. Alastair I.M. Rae, Quantum Physics: A Beginner's Guide, One world Publications, Revised Edition, 2005
5. Eleanor G. Rieffel, Wolfgang H. Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011
6. Leonard Susskind, Art Friedman, Quantum Mechanics: The Theoretical Minimum, Basic Books, 2014
7. Bruce Rosenblum, Fred Kuttner, Quantum Enigma: Physics Encounters Consciousness, Oxford University Press, 2nd Edition, 2011

COURSE OUTCOMES:

1. Explain core quantum principles in a non-mathematical manner.
2. Compare classical and quantum information systems
3. Identify theoretical issues in building quantum computers
4. Discuss quantum communication and computing concepts
5. Recognize applications, industry trends, and career paths in quantum technology

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209A) ENTREPRENEURSHIP ESSENTIALS (AC-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I FOUNDATIONS OF ENTREPRENEURSHIP**

Introduction to Entrepreneurship, Case Studies: Dhirubhai Ambani & Sofia, Myths and Realities about Entrepreneurship, Entrepreneurial Qualities and Mindset, Mission and Vision Development, Why Start-ups Fail Common Pitfalls and Lessons Learned

UNIT-II BUSINESS MODELS AND STRATEGIC PLANNING

Value Proposition and Opportunity Identification, Business Model Canvas and Business Model Generation, Competitive Advantage and Lean Start-up Methodology, Team Formation and Early Recruitment, Legal Forms of Business and Organizational Structure.

UNIT-III MARKETING, FINANCE, AND BUSINESS PLANNING

Marketing Management Principles for Start-ups, Market Research: Methods, Data Analysis, and Case Studies, Financial Statements: P&L, Balance Sheet, and Cash Flow, Cost-Volume-Profit Analysis and Break-even Analysis, Capital Budgeting and Financial Decision Making, Business Plan Preparation and Pitching Techniques

UNIT-IV INNOVATION, FUNDING, AND LEGAL FRAMEWORK

Innovation Strategies: Design Thinking, TRIZ, Open Innovation, Government Incentives and Support Systems for Entrepreneurs, Incubation and Acceleration Programs, Funding Sources: Bootstrapping, Crowdfunding, Angel Investors, Venture Capital, Debt Financing, Due Diligence and Project Cost Management, Legal Aspects: IPR, GST, and Labor Laws

UNIT-V GROWTH, HUMAN RESOURCE, AND RISK MANAGEMENT

Growth Hacking and Business Scaling Strategies, Human Resource Management in Start-ups, Negotiation Skills and Leadership Development, Pivoting Strategies and Entrepreneurial Case Studies, Risk Assessment and Strategic Management for Start-ups, Success and Failure Factors in Entrepreneurial Ventures

TEXT BOOKS:

1. Effective Entrepreneurial Management: Strategy, Planning, Risk Management, and Organization - Robert D. Hisrich Veland Ramadani, Springer (2017)
2. Entrepreneurship- Theory, Process Practice by Kuratko &Hodgetts, Thompson South-Western Publication
3. Entrepreneurship by Robert D. Hisrich (Edition-9)



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Explain the stages in the entrepreneurial venture life-cycle and the critical decisions involved in each stage.
2. Identify, evaluate, and select potential business opportunities using structured entrepreneurial frameworks.
3. Demonstrate the ability to prepare basic financial statements, project reports, and feasibility analyses for start-up ventures
4. Apply management principles marketing, HR, and strategic planning in designing and managing small or emerging enterprises.
5. Analyze funding options, risk factors, and legal aspects to support sustainable and ethical entrepreneurial ventures

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209B) PEDAGOGY STUDIES (AC-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

UNIT-I INTRODUCTION AND METHODOLOGY

Aims and Rationale, Policy Background, Conceptual Framework and Terminology, Theories of Learning, Curriculum, Teacher Education, Conceptual Framework, Research Questions, Overview of Methodology, and Searching.

UNIT-II THEMATIC OVERVIEW

Pedagogical Practices being used by teachers in formal and informal classrooms in developing countries, Curriculum, and Teacher Education.

UNIT-III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES, METHODOLOGY FOR THE IN DEPTH STAGE

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the echo curriculum and guidance materials best support effective pedagogy. Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers attitudes and beliefs and Pedagogic strategies.

UNIT-IV PROFESSIONAL DEVELOPMENT

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V RESEARCH GAPS AND FUTURE DIRECTIONS

Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

TEXT BOOKS:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M(2004) Curricular reform in schools: The importance of evaluation, Journal of 3. Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K(2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count International Journal Educational Development, 33 (3): 272-282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education.
6. Oxford and Boston: Blackwell. Chavan M (2003) Read India: A mass scale, rapid, learning to read campaign.
www.pratham.org/images/resource%20working%20paper%202.pdf.



SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Understand and explain the foundational aspects of education including aims, rationale, policy background, theories of learning, curriculum design, and teacher education methodologies.
2. Identify and analyze various pedagogical practices adopted in formal and informal classroom settings in developing countries, and evaluate their implications for curriculum and teacher education.
3. Evaluate evidence-based research on the effectiveness of pedagogical practices and examine how teacher education, curriculum, and professional materials can support effective pedagogy through a strong theoretical and methodological framework.
4. Assess and apply principles of professional development, focusing on classroom alignment, peer and community support, and overcoming barriers such as limited resources and large class sizes.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209C) YOGA FOR STRESS MANAGEMENT (AC-II)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I DEFINITIONS OF EIGHT PARTS OF YOGA (ASHTANGA)**

Definitions and explanation of the eight parts of Yog (Ashtanga): Yama, Niyama, Asana, Pranayama, Pratyahara, Dharana, Dhyana, and Samadhi. Understanding the holistic approach of Ashtanga Yog in managing stress and achieving mental balance.

UNIT-II YAM AND NIYAM

Detailed study of Yam and Niyam their meaning, importance, and practical application in daily life. Understanding how ethical and personal disciplines help in stress reduction and personality development.

UNIT-III DO'S AND DON'TS IN LIFE

i) Yam (Do's): Ahimsa, Satya, Astheya, Brahmacharya, and Aparigraha. ii) Niyam (Don'ts): Shaucha, Santosha, Tapa, Swadhyaya, and Ishwar Pranidhana. Emphasis on self-discipline, moral conduct, and positive thinking as tools for peaceful living and stress control.

UNIT-IV ASAN AND PRANAYAM

Introduction to Asanas (Postures) and Pranayam (Breathing Techniques). Importance of physical postures and controlled breathing in maintaining physical fitness, mental calmness, and emotional stability.

UNIT-V VARIOUS YOGA POSES AND THEIR BENEFITS FOR MIND & BODY

i) Study of various Yog poses and their specific benefits for the mind and body.
ii) Regularization of breathing techniques and their physiological and psychological effects.
Types of Pranayam: Anulom Vilom, Bhastrika, Kapalbhathi, Bhramari, and others.

TEXT BOOKS:

1. Yogic Asanas for Group Training-Part-I: Janardan Swami Yoga bhyasi Mandal, Nagpur
2. Rajayogaor conquering the Internal Nature by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

REFERENCE BOOKS:**e-Resources and Digital Material:****COURSE OUTCOMES:**

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209D) CONSTITUTION OF INDIA (AC-II)

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To help students understand the basic features, principles, and structure of the Indian Constitution.
2. To familiarize students with the fundamental rights, duties, and directive principles that form the foundation of Indian democracy
3. To understand the roles and responsibilities of the Union and State governments, and the functioning of the judiciary
4. To develop awareness of the constitutional provisions related to governance, policy-making, and administration
5. To inspire students to be responsible citizens by understanding their constitutional rights and duties

UNIT-I INTRODUCTION TO THE CONSTITUTION OF INDIA

Historical Background-Making of the Constitution-Preamble to the Constitution-Salient Features of the Constitution-The Union and Its Territory-Citizenship Fundamental Rights and Fundamental Duties Directive Principles of State Policy.

UNIT-II UNION GOVERNMENT AND ITS ADMINISTRATION STRUCTURE OF THE INDIAN UNION –

Structure of the Indian Union – Powers and Functions of the President, Vice President, Prime Minister, Council of Ministers, and Parliament – Cabinet Committees – Role and Responsibilities of the Prime Minister's Office – Lok Sabha and Rajya Sabha: Composition, Powers, and Functions.

UNIT-III STATE GOVERNMENT AND ITS ADMINISTRATION GOVERNOR

Governor Chief Minister Council of Ministers State Legislature High Courts and Subordinate Courts Special Status of Jammu & Kashmir and other States Centre-State Relations Administration of Union Territories.

UNIT-IV LOCAL GOVERNANCE AND CONSTITUTIONAL BODIES

Panchayati Raj Institutions: 73rd and 74th Constitutional Amendments – Urban and Rural Local Bodies – Election Commission – Union and State Public Service Commissions – Finance Commission – Comptroller and Auditor General of India – Attorney General and Advocate General.

UNIT-V CONSTITUTIONAL AMENDMENTS AND EMERGENCY PROVISIONS

Amendment Procedure Major Amendments and Their Significance Emergency Provisions: National, State, and Financial Emergencies Judicial Review and Independence of Judiciary Right to Information Act Role of the Constitution in Nation Building and Citizen Empowerment.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Dr. J. N. Pandey, The Constitutional Law of India, Central Law Agency, 2022.
2. D.D. Basu, Introduction to the Constitution of India, LexisNexis, 25th Edition, 2021.
3. M. Laxmi kanth, Indian Polity, McGraw Hill Education, 7th Edition, 2023.
4. Granville Austin, The Indian Constitution: Cornerstone of a Nation, Oxford University Press, 2014.
5. Subhash Kashyap, Our Constitution: An Introduction to India's Constitution and Constitutional Law, National Book Trust, India, 2018.

REFERENCE BOOKS:

COURSE OUTCOMES:

1. Understand the key elements, philosophy, and evolution of the Indian Constitution.
2. Describe the structure and functioning of the Union, State, and Local Governments.
3. Analyze the importance of Fundamental Rights, Duties, and Directive Principles in ensuring social justice
4. Recognize the role of various constitutional bodies and their impact on governance
5. Develop a sense of civic responsibility, constitutional awareness, and commitment to national integrity and harmony.



**M. Tech (VLSISD Branch)
Course Structure
III-Semester**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN****M.Tech. III Sem. - Course Structure**

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				L	T	P	C	IM	EM	T
1	25D57301A	PE	BI-CMOS TECHNOLOGY AND APPLICATIONS (PE-V)	3	0	0	3	40	60	100
2	25D57301B	PE	OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN (PE-V)	3	0	0	3	40	60	100
3	25D57301C	PE	VLSI DESIGN FLOW- RTL TO GDS (PE-V)	3	0	0	3	40	60	100
4	25D57301D	PE	SOC ARCHITECTURE (PE-V)	3	0	0	3	40	60	100
5	25D06301	OE	IOT AND ITS APPLICATIONS (OE-I)	3	0	0	3	40	60	100
6	25D20301	OE	GREEN BUILDINGS (OE-I)	3	0	0	3	40	60	100
7	25D93301	OE	ROAD SAFETY ENGINEERING (OE-I)	3	0	0	3	40	60	100
8	25D91301	OE	INDUSTRIAL SAFETY (OE-I)	3	0	0	3	40	60	100
9	25D58101	OE	ADVANCED DATA STRUCTURES & ALGORITHMS (OE-I)	3	0	0	3	40	60	100
10	25D58305	OE	CLOUD COMPUTING (OE-I)	3	0	0	3	40	60	100
11	25D13305	OE	AI TOOLS (OE-I)	3	0	0	3	40	60	100
12	25D95301	OE	PHOTOVOLTAIC SYSTEMS (OE-I)	3	0	0	3	40	60	100
13	25D15301	OE	INTEGRATED PRODUCT DESIGN AND DEVELOPMENT (OE-I)	3	0	0	3	40	60	100
14	25D99301A	OE	ADVANCED NUMERICAL METHODS AND COMPUTATIONAL MATHEMATICS (OE-I)	3	0	0	3	40	60	100
15	25D99301B	OE	MATHEMATICS FOR MACHINE LEARNING AND DATA SCIENCE (OE-I)	3	0	0	3	40	60	100
16	25D99301C	OE	STATISTICAL LEARNING THEORY AND MATHEMATICAL FOUNDATIONS OF AI (OE-I)	3	0	0	3	40	60	100
17	25D99301D	OE	CHEMISTRY OF NANOMATERIALS AND APPLICATIONS IN ENGINEERING (OE-I)	3	0	0	3	40	60	100
18	25D99301E	OE	PHOTONICS FOR ENGINEERS (OE-I)	3	0	0	3	40	60	100
19	25D57302	PR	DISSERTATION PHASE – I	0	0	20	10	100	00	100
20	25D57303	PR	INDUSTRY INTERNSHIP	0	0	0	2	100	00	100
21	25D57304	PR	CO- CURRICULAR ACTIVITIES	0	0	0	1	100	00	100



**M. Tech (VLSISD Branch)
III-Semester
Syllabus**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D57301A) BI-CMOS TECHNOLOGY AND APPLICATIONS (PE-V)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To demonstrate in-depth knowledge in BiCMOS Technology.
2. To analyze complex engineering problems critically for conducting research in BiCMOS Technology.
3. To solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. To realize different digital circuits using BiCMOS Technology

UNIT-I BICMOS PROCESS TECHNOLOGY

CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS and Bipolar Technologies, BiCMOS Technology, BiCMOS Design Rules.

UNIT-II DEVICE DESIGN CONSIDERATIONS

Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations. BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling

UNIT-III DEVICE MODELING

Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICE Models of the MOS Transistor, Analytical Model for Short-Channel MOS Devices. Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-Moll Model, Bipolar Models in SPICE.

UNIT-IV BICMOS DIGITAL INTEGRATED CIRCUITS

BiMOS Totem-Pole Inverter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates

UNIT-V BICMOS DIGITAL CIRCUIT APPLICATIONS

Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

TEXT BOOKS:

1. Sherif H.K. Embabi, Abdellatif Bellaouar & Mohamed I. Elmasry —Digital BiCMOS Integrated Circuit Design|| Springer Science+Business Media, LLC.
2. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2. James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press
3. KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science

COURSE OUTCOMES:

1. Demonstrate in-depth knowledge in BiCMOS Technology.
2. Analyze complex engineering problems critically for conducting research in BiCMOS Technology.
3. Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. Realize different digital circuits using BiCMOS Technology

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

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L	T	P	C
3	0	0	3

(25D57301B) OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN (PE-V)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand basics of statistical modeling
2. To analyze performance of CMOS circuits with respect to power, area and speed
3. To acquire complete knowledge regarding the various algorithms used for optimization of power and area

UNIT-I STATISTICAL MODELING

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT-II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III CONVEX OPTIMIZATION

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wiresizing, Approximation and fitting-Monomial fitting, Max monomial fitting, Polynomial fitting

UNIT-IV GENETIC ALGORITHM

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm Taxonomy Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS Standard cell placement GASP algorithm-unified algorithm.

UNIT-V GA ROUTING PROCEDURES AND POWER ESTIMATION

Global routing-FPGA technology mapping circuit generation-test generation in a GA frame work-test generation procedures, Power estimation application of GA Standard cell placement - GA for ATG-problem encoding-fitness function-GA Vs Conventional algorithm.



SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E. Mrudnick, Prentice Hall,1998.

REFERENCE BOOKS:

1. Convex Optimization- Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004

COURSE OUTCOMES:

1. Understand basics of statistical modeling
2. Analyze performance of CMOS circuits with respect to power, area and speed
3. Acquire complete knowledge regarding the various algorithms used for optimization of power and area

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D57301C) VLSI DESIGN FLOW- RTL TO GDS (PE-V)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I INTRODUCTION TO INTEGRATED CIRCUITS AND VLSI DESIGN FLOW**

Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit, Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis. Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; Post GDS Processes

UNIT-II HARDWARE MODELING AND VERIFICATION

Hardware Modeling: Introduction to Verilog, Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog. RTL Synthesis: Verilog Constructs to Hardware, Logic Optimization: Definitions, Two level logic optimization

UNIT-III LOGIC OPTIMIZATION AND FORMAL VERIFICATION

Logic Optimization: Multi-level logic optimization, FSM Optimization, Formal Verification: Introduction, Formal Engines: BDD, SAT Solver. Formal Verification: Model Checking, Combinational Equivalence Checking, Technology Library: Delay models of Combinational and Sequential Cells

UNIT-IV TIMING ANALYSIS AND TECHNOLOGY MAPPING

Static Timing Analysis: Synchronous Behavior, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations Constraints: Clock, I/O, Timing Exceptions, Technology Mapping, Timing-driven Optimizations

UNIT-V POWER ANALYSIS, DESIGN FOR TEST, AND PHYSICAL DESIGN

Power Analysis, Power-driven Optimizations, Design for Test: Basics and Fault Models, Scan Design Methodology Design for Test: ATPG, BIST, Basic Concepts for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files Chip Planning: Partitioning, Floor planning, Power Planning, Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews, Routing: Global and Detailed, Optimizations, Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off



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TEXT BOOKS:

1. Sneh Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023 (expected)
<https://www.cambridge.org/highereducation/books/introduction-to-vlsi-design-flow/93E6832E63FE6B795181D6D67B552333#overview>
2. M.J.S. Smith, "Application-specific integrated circuits", Addison-Wesley, 1997
3. L. Lavagno, I. L. Markov, G. Martin, and L. K. Scheffer (Editors), "Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology", CRC Press, 2016
4. S. Palnitkar, "Verilog HDL: a guide to digital design and synthesis", Pearson Education India, 2003
5. J. Bhasker and R. Chadha, "Static timing analysis for nanometer designs: A practical approach", Springer Science Business Media,

REFERENCE BOOKS:

1. G. D. Micheli, "Synthesis and optimization of digital circuits", McGraw-Hill Higher Education, 1994
2. M. Bushnell and V. Agrawal, "Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits", Springer Science & Business Media, 2004

COURSE OUTCOMES:

1. Students will understand the fundamental concepts of integrated circuits, VLSI design flow, and the methodologies involved in pre-RTL and RTL to GDS implementation.
2. Students will be able to model hardware using Verilog, perform functional verification through simulation, and understand RTL synthesis and two-level logic optimization
3. Students will learn advanced logic optimization techniques and understand formal verification methods and delay models for combinational and sequential cells.
4. Students will be able to perform static timing analysis, understand timing requirements and constraints, and apply technology mapping and timing-driven optimizations

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D57301D) SOC ARCHITECTURE (PE-V)

Course Category	Professional Elective (PE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the basics related to SoC architecture and different approaches related to SoC Design.
2. To select an appropriate robust processor for SoC Design
3. To select an appropriate memory for SoC Design.
4. To realize real time case studies

UNIT-I INTRODUCTION TO THE SYSTEM APPROACH

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory & Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II PROCESSORS

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT-III MEMORY DESIGN FOR SOC

Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV INTERCONNECT, CUSTOMIZATION AND CONFIGURABILITY

Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V APPLICATION STUDIES / CASE STUDIES

SOC Design approach; AES-algorithms, Design and evaluation; Image compression-JPEG compression.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2nd Edition, 2000, Addison Wesley Professional

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

COURSE OUTCOMES:

1. Understand the basics related to SoC architecture and different approaches related to SoC Design
2. Select an appropriated robust processor for SoC Design
3. Select an appropriate memory for SoC Design.
4. Realize real time case studies

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D06301) IOT AND ITS APPLICATIONS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To implement the state of the Architecture of an IOT.
4. To compare IOT Applications in Industrial & real world.
5. To demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT-I FUNDAMENTALS OF IOT

Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects. IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT-II IOT PROTOCOLS

IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT-III DESIGN AND DEVELOPMENT

Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT-IV DESIGN METHODOLOGY, EMBEDDED COMPUTING LOGIC, MICROCONTROLLER, SYSTEM ON CHIPS, IOT SYSTEM BUILDING BLOCKS, ARDUINO, BOARD DETAILS, IDE PROGRAMMING, RASPBERRY PI, INTERFACES AND RASPBERRY PI WITH PYTHON PROGRAMMING.

Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT-V CASE STUDIES/INDUSTRIAL APPLICATIONS

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015

REFERENCE BOOKS:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence, Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

COURSE OUTCOMES:

1. Apply the Knowledge in IOT Technologies and Data management.
2. Determine the values chains Perspective of M2M to IOT.
3. Implement the state of the Architecture of an IOT.
4. Compare IOT Applications in Industrial & real world
5. Demonstrate knowledge and understand the security and ethical issues of an IOT

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D20301) GREEN BUILDINGS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the fundamental concepts of green buildings, their necessity, and sustainable features. (Understanding - Level 2)
2. To analyze green building concepts, rating systems, and their benefits in India. (Analyzing - Level 4)
3. To apply green building design principles, energy efficiency measures, and renewable energy sources. (Applying - Level 3)
4. To evaluate air conditioning systems, HVAC designs, and energy modeling for sustainable buildings. (Evaluating - Level 5)
5. To assess material conservation strategies, waste management, and indoor environmental quality in green buildings. (Evaluating - Level 5)

UNIT-I INTRODUCTION TO GREEN BUILDING

Necessity of Green Buildings, Benefits of Green Buildings, Green Building Materials and Equipment in India, Key Requisites for Constructing a Green Building, Important Sustainable Features for Green Buildings.

UNIT-II GREEN BUILDING CONCEPTS AND PRACTICES

Indian Green Building Council, Green Building Movement in India, Benefits Experienced in Green Buildings, Launch of Green Building Rating Systems, Residential Sector, Market Transformation; Green Building Opportunities and Benefits: Opportunities of Green Buildings, Green Building Features, Material and Resources, Water Efficiency, Optimum Energy Efficiency, Typical Energy-Saving Approaches in Buildings, LEED India Rating System, and Energy Efficiency.

UNIT-III GREEN BUILDING DESIGN – INTRODUCTION,

Reduction in Energy Demand, Onsite Sources and Sinks, Maximizing System Efficiency, Steps to Reduce Energy Demand and Use Onsite Sources and Sinks, Use of Renewable Energy Sources, Eco-friendly Captive Power Generation for Factories, Building Requirements.

UNIT-IV AIR CONDITIONING – INTRODUCTION,

CII Godrej Green Business Centre, Design Philosophy, Design Interventions, Energy Modeling, HVAC System Design, Chiller Selection, Pump Selection, Selection of Cooling Towers, Selection of Air Handling Units, Pre-cooling of Fresh Air, Interior Lighting Systems, Key Features of the Building, Eco-friendly Captive Power Generation for Factories, Building Requirements.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V MATERIAL CONSERVATION

Handling of Non-Process Waste, Waste Reduction During Construction, Materials with Recycled Content, Local Materials, Material Reuse, Certified Wood, Rapidly Renewable Building Materials and Furniture. Indoor Environment Quality and Occupational Health – Air Conditioning, Indoor Air Quality, Sick Building Syndrome, Tobacco Smoke

TEXT BOOKS:

1. Handbook on Green Practices published by Indian Society of Heating Refrigerating and Air conditioning Engineers, 2009
2. Green Building Hand Book by Tomwoolley and Samkimings, 2009.

REFERENCE BOOKS:

1. Complete Guide to Green Buildings by Trish riley
2. Standard for the design for High Performance Green Buildings by Kent Peterson, 2009
3. Energy Conservation Building Code –ECBC-2020, published by BEE

COURSE OUTCOMES:

1. Understand the importance of green buildings, their necessity, and sustainable features. (Understanding - Level 2)
2. Analyze various green building practices, rating systems, and their impact on environmental sustainability. (Analyzing - Level 4)
3. Apply principles of green building design to enhance energy efficiency and incorporate renewable energy sources. (Applying - Level 3)
4. Evaluate HVAC systems, energy-efficient air conditioning techniques, and their role in sustainable building design. (Evaluating - Level 5)
5. Assess material conservation techniques, waste reduction strategies, and indoor air quality management in green buildings. (Evaluating - Level 5)

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M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D93301) ROAD SAFETY ENGINEERING (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Discusses the fundamentals causes of road accidents & some of the statistical methods to analyze the traffic safety.
2. The accident investigation and risk management are dealt.
3. Introduction of Road Safety as an integral part of Road Design is emphasized.

UNIT-I ACCIDENT INVESTIGATIONS AND RISK MANAGEMENT

Collection of Accident Data, Assessment of Road Safety, Methods to Identify and Prioritize Hazardous Locations and Elements, Determine Possible Causes of Crashes, Crash Reduction Capabilities and Countermeasures, Effectiveness of Safety Design Features, Accident Reconstruction, Condition and Collision Diagram

UNIT-II TRAFFIC ENGINEERING STUDIES;

Statistical Methods In Traffic Safety Analysis –Regression Methods, Poisson Distribution, Chi- Squared Distribution, Statistical Comparisons- Traffic Management Measures and Their Influence On Accident Prevention.

UNIT-III ROAD SAFETY IN ` TRANSPORT PLANNING AND GEOMETRIC DESIGN

Vehicle and Human Characteristics, Road Design and Safety Elements, Redesigning Junctions, Cross Section Improvements, Traffic Control, Traffic Calming Measures, Road Safety Furniture

UNIT-IV ROLE OF SIGNS AND MARKINGS IN ` SAFETY

Types of Signs – Design Specifications – Guidelines for Installation – Role of Signs in `Safety; Types of Road Markings – Design Specifications – Role of Road Markings in `Safety.

UNIT-V TRAFFIC MANAGEMENT SYSTEMS FOR SAFETY

Road Safety Audits and Tools for Safety Management Systems, Road Safety Audit Process, Road Safety Improvement Strategies, ITS and Safety.

TEXT BOOKS:

1. Traffic Engineering and Transportation Planning – L.R. Kadiyali, Khanna Publishers
2. Fundamentals of Transportation Engineering - C.S. Papacostas, Prentice Hall India.
3. Road Safety by NCHRP



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Transportation Engineering – An Introduction, C. Jotin Khisty, B. Kent Lall
2. Fundamentals of Traffic Engineering, Richardo G Sigua
3. Handbook of Road Safety Measures, Second Edition, Rune Elvik, Alena Hoyer, Truls Vaa, Michael Sorenson

COURSE OUTCOMES:

1. To understand the basic causes of road accidents
2. To conduct accident investigations and identify black spots
3. To design & plan road geometrics incorporating road safety
4. To understand the importance of Road Signs and Markings
5. To conduct Road Safety Audit

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M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D91301) INDUSTRIAL SAFETY (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To list out important legislations related to health, Safety and Environment
2. To list out requirements mentioned in factories act for the prevention of accidents
3. To understand the health and welfare provisions given in factories act
4. To analyze the fault tracing in the industry safety
5. To apply the procedures of periodic and preventive maintenance methods in the industry safety

UNIT-I INDUSTRIAL SAFETY

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc., Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT-II FUNDAMENTALS OF MAINTENANCE ENGINEERING

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment

UNIT-III WEAR AND CORROSION AND THEIR PREVENTION

Wear- types, causes, effects, wear reduction methods, lubricants- types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods

UNIT-IV FAULT TRACING

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault-finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.



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UNIT-V PERIODIC AND PREVENTIVE MAINTENANCE

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

TEXT BOOKS:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

REFERENCE BOOKS:

1. Pump-hydraulic Compressors, Audels, McGraw Hill Publication
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London

COURSE OUTCOMES:

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L	T	P	C
3	0	0	3

(25D58101) ADVANCED DATA STRUCTURES & ALGORITHMS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Introduce fundamental data structures including linked lists, stacks, queues, trees, graphs, dictionaries, and hashing techniques
2. Develop algorithmic skills for designing and analyzing searching, sorting, and traversal methods
3. Teach implementation of priority queues, binary search trees, and balanced trees (AVL, Red Black, Splay, B-Trees).
4. Enable students to select and apply appropriate data structures for solving computational problems efficiently
5. Foster understanding of the performance analysis and comparative evaluation of data structures and algorithms.

UNIT-I INTRODUCTION

Introduction to Data Structures, Singly Linked Lists, Doubly Linked Lists, Circular Lists-Algorithms. Stacks and Queues: Algorithm Implementation using Linked Lists.

UNIT-II SEARCHING AND SORTING

Linear and Binary Search Methods, Sorting: -Basic sorting techniques, Radix Sort, Bucket Sort, Shell Sort Trees- Binary trees, Properties, Representation and Traversals, Expression Trees (Infix, prefix, postfix). Graphs-Basic Concepts, Storage structures and Traversals.

UNIT-III DICTIONARIES AND HASHING

Dictionaries: Definition, Dictionary Abstract Data Type, Implementation of Dictionaries. Hashing: Review of Hashing, Hash Function, Collision Resolution Techniques in Hashing, Separate Chaining, Open Addressing, Linear Probing, Quadratic Probing, Double Hashing, Rehashing, Extendible Hashing

UNIT-IV PRIORITY QUEUES

Definition, ADT, Realizing a Priority Queue Using Heaps, Definition, Insertion, Deletion, Search Trees- Binary Search Trees, Definition, ADT, Implementation, Operations- Searching, Insertion, Deletion.

UNIT-V SEARCH TREES-

AVL Trees, Definition, Height of AVL Tree, Operations-, Insertion, Deletion and Searching, Introduction to Red-Black and Splay Trees, B-Trees, Height of B-Tree, Insertion, Deletion and Searching, Comparison of Search Trees.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Data Structures: A Pseudo Code Approach, 2/e, Richard F. Gilberg, Behrouz A. Forouzon and Cengage
2. Data Structures, Algorithms and Applications in java, 2/e, SartajSahni, University Press

REFERENCE BOOKS:

1. Data Structures and Algorithm Analysis, 2/e, Mark Allen Weiss, Pearson.
2. Data Structures and Algorithms, 3/e, Adam Drozdek, Cengage
3. C and Data Structures: A Snap Shot Oriented Treatise Using Live Engineering Examples, N.B. Venkateswarulu, E.V. Prasad and S Chand & Co.

COURSE OUTCOMES:

1. Implement and manipulate linear data structures like singly/doubly linked lists, circular lists, stacks, and queues using dynamic memory allocation.
2. Apply and analyze searching and sorting algorithms including linear, binary search, bubble, selection, insertion, quick, and merge sort.
3. Design and implement dictionaries and hashing techniques to efficiently store and retrieve data.
4. Construct and operate on trees and priority queues, performing insertion, deletion, and traversal operations.
5. Compare and implement balanced search trees (AVL, Red-Black, Splay, B-Trees) for optimized data access and storage.

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D58305) CLOUD COMPUTING (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Analyze the trade-offs between deploying applications in the cloud and over the local infrastructure. Compare the advantages and disadvantages of various cloud computing platforms.
2. Investigate how a global storage solution can be optimized so that it can be delivered successfully from the cloud
3. Evaluate information storage management design in a cloud environment and how it relates to the business objectives of an organization
4. Analyze how best to provide reliable access to information both locally and remotely using storage technologies
5. Critically appraise the opportunities and challenges of information management in complex business environments.

UNIT-I

Definition, characteristics, components, Cloud service provider, the role of networks in Cloud computing, Cloud deployment models- private, public & hybrid, Cloud service models, multitenancy, Cloud economics and benefits, Cloud computing platforms - IaaS: Amazon EC2, PaaS: Google App Engine, Microsoft Azure, SaaS.

UNIT-II

Virtualization concepts, Server virtualization, Storage virtualization, Storage services, Network virtualization, Service virtualization, Virtualization management, Virtualization technologies and architectures, virtual machine, Measurement and profiling of virtualized applications. Hypervisors: KVM, Xen, VMware hypervisors and their features

UNIT-III

Relational databases, Cloud file systems: GFS and HDFS, Bigtable, HBase and Dynamo. MapReduce and extensions: Parallel computing, the map -Reduce model, Parallel efficiency of Map Reduce

UNIT-IV

Cloud security fundamentals, Vulnerability assessment tool for cloud, Privacy and Security in cloud. Cloud computing security architecture: General Issues, Trusted Cloud computing, Secure Execution Environments and Communications, Micro - architectures; Identity Management and Access control, Autonomic security.

UNIT-V

Issues in cloud computing Implementing real time application over cloud platform, Issues in Inter - cloud environments, QoS Issues in Cloud, Dependability, data migration, streaming in Cloud. Quality of Service (QoS) monitoring in a Cloud computing environment. Cloud Middleware.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Enterprise Cloud Computing by Gautam Shroff, Cambridge publication
2. Gautam Shroff, —Enterprise Cloud Computing Technology Architecture Applications||, Cambridge University Press; 1 edition, [ISBN: 978-0521137355], 2010.

REFERENCE BOOKS:

1. Cloud Security by Ronald Krutz and Russell Dean Vines, Wiley -India
2. Dr. Kumar Saurabh, —Cloud Computing||, Wiley Publication
3. Dimitris N. Chorafas, —Cloud Computing Strategies|| CRC Press; 1 edition [ISBN: 1439834539], 2010
4. Toby Velte, Anthony Velte, Robert Elsenpeter, —Cloud Computing, A Practical Approach|| McGraw Hill Osborne Media; 1 edition [ISBN: 0071626948], 200
4. Rajkumar Buyya, James Broberg, Andrzej M. Goscinski, —Cloud Computing: Principles and Paradigms||, Wiley Publication, 2011
5. Tim Mather, Subra Kumaraswamy, Shahed Latif, —Cloud Security and Privacy: An Enterprise Perspective on Risks and Compliance||, O'Reilly Media Inc, 2009

COURSE OUTCOMES:

1. Deploy applications over commercial cloud computing infrastructures such as Amazon Web Services, Windows Azure, and Google App Engine.
2. Program data intensive parallel applications in the cloud
3. Analyze the performance, scalability, and availability of the underlying cloud technologies and software.
4. Identify security and privacy issues in cloud computing.
5. Solve a real-world problem using cloud computing through group collaboration.

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M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D13305) AI TOOLS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Explain the fundamentals and evolution of AI tools
2. Use AI tools for text, language, and communication tasks
3. Apply AI tools for image, audio, and video generation
4. Utilize AI tools for coding, research, and productivity enhancement
5. Analyze ethical, security, and application-oriented aspects of AI tools

UNIT-I INTRODUCTION TO AI TOOLS

Definition of Artificial Intelligence, Evolution of AI and Intelligent Systems, Categories of AI Tools (Generative, Analytical, Assistive), Rule-based vs Learning-based AI Tools, Overview of Machine Learning & Deep Learning Tools, AI Tool Ecosystem (OpenAI, Google, Meta, Microsoft), Cloud-based AI Tools, Future Trends in AI Tool Development

UNIT-II TEXT & LANGUAGE AI TOOLS

Natural Language Processing (NLP) Basics, ChatGPT – Architecture and Capabilities, Prompt Engineering Concepts, AI Tools for Content Writing, AI Tools for Email, Resume & Report Generation, AI-based Translation and Summarization Tools, AI Chatbots and Virtual Assistants, Limitations and Bias in Language AI Tools.

UNIT-III

Image, Audio & Video AI Tools:

Tools for Graphic Design & Posters, Text-to-Speech AI Tools (Eleven Labs, Google TTS), Speech-to-Text AI Tools, AI-based Video Creation Tools, Avatar and Animation AI Tools, Applications in Media, Education & Healthcare

UNIT-IV AI TOOLS FOR CODING, RESEARCH & PRODUCTIVITY

AI Tools for Programming Assistance, Code Generation and Debugging using AI, AI Tools for Data Analysis, AI Tools for Research Paper Writing, AI Tools for Literature Survey and Citations, AI in Project Management, AI Tools for Presentation Creation, AI Tools for Automation and Workflow Optimization

UNIT-V ETHICAL, SECURITY & APPLIED AI TOOLS

Ethical Issues in AI Tool Usage, Data Privacy and Security Concerns, AI Tool Regulations and Policies, AI Tools in Education, AI Tools in Healthcare, AI Tools in Finance and Business, AI Tools in Smart Cities and Governance, Responsible and Sustainable AI Practices



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, 4th Edition, Pearson Education, 2021.
2. Michael Miller, AI for Everyone, Pearson, 2020.
3. Liam Ottley, Artificial Intelligence for Business, Wiley, 2022.

REFERENCE BOOKS:

1. Kai-Fu Lee, AI Superpowers: China, Silicon Valley, and the New World Order, Houghton Mifflin Harcourt, 2018.
2. Bernard Marr, Artificial Intelligence in Practice, Wiley, 2020.
3. Ethical Guidelines for Trustworthy AI, European Commission, 2019.

COURSE OUTCOMES:

1. Understand the fundamentals and evolution of AI tools
2. Explore popular AI tools for text, image, video, and code generation
3. Apply AI tools in education, research, and industry use cases
4. Analyze ethical, security, and societal implications of AI tools
5. Develop practical skills to effectively use AI tools for productivity and innovation

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D95301) PHOTOVOLTAIC SYSTEMS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To introduce photovoltaic systems
2. To deal with various technologies of solar PV cells.
3. To understand details about manufacture, sizing and operating techniques.
4. To have knowledge of design considerations.

UNIT-I SOLAR ENERGY

Sun and Earth, Solar Spectrum, Solar Geometry, Solar radiation on horizontal and inclined planes, Instruments for measurement of solar radiation, Solar cell, Equivalent circuit, V-I characteristics, Performance improvement.

UNIT-II SOLAR CELLS

Manufacture of Solar Cells-Technologies, Design of Solar cells, Photovoltaic modules, Design requirements, Encapsulation systems, Manufacture, Power rating, Hotspot effect, Design qualifications.

UNIT-III PROTECTION AND MEASUREMENTS

Flat plate arrays, Support structures, Module interconnection and cabling, Lightning protection, Performance measurement using natural sun light and simulator, Determination of temperature coefficients, Internal series resistance, Curve correction factor.

UNIT-IV PHOTOVOLTAIC SYSTEMS

Photovoltaic systems, Types, General design considerations, System sizing, Battery sizing, Inverter sizing, Design examples, Balance of PV systems.

UNIT-V MAXIMUM POWER POINT TRACKERS

Maximum power point trackers, Perturb and observe, Incremental conductance method, Hill climbing method, Hybrid and complex methods, Data based and other approximate methods, Instrument design, Other MPP techniques, Grid interactive PV system.

TEXT BOOKS:

1. F.C. Treble, —Generating electricity from Sun||, Pergamon Press.
2. A.K. Mukherjee, Nivedita Thakur, || Photovoltaic systems: Analysis and design||, PHI, 2011.

REFERENCE BOOKS:

1. C.S. Solanki, || Solar Photo voltaic's: Fundamentals, Technologies and applications||, PHI, 2009.

COURSE OUTCOMES:

1. Identify photovoltaic system components and system types. L2
2. Calculate electrical energy and power. L2
3. Correctly size system components, design considerations of solar equipment. L3
4. Design a basic grid-tie PV system. L5

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M.Tech. III Sem.

L	T	P	C
3	0	0	3

**(25D15301) INTEGRATED PRODUCT DESIGN AND DEVELOPMENT
(OE-I)**

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To know the design concepts, product development planning and customer requirements
2. To generate the concept using creative problem solving methods, concept generation and testing
3. To understand product teardown, specifications, portfolios and Architecture, configurations and detailed design with prototyping
4. To acquaint DFN process and know design aspects for risk, reliability and safety and environments
5. To do industrial design, intellectual property and robust design and product development economics

UNIT-I PRODUCT DEVELOPMENT CONCEPTS

Design Concepts: Design process – Considerations of a good design – Description of good design process – Design codes and standards. Product Development and Planning Process: Characteristics and challenges of product development – Concept development – Generic product development – Product development process flows –Tyco product development – Product development organizations – Organizational structure and design – Product and process cycles – Technological innovation – Structure of opportunity – Opportunity identification – Product planning process – Types of product development

UNIT-II CONCEPT SELECTION, GENERATION AND TESTING

Concept Generation: Activity – Concept generation process – Creativity and problem solving – Creative thinking methods and design – Functional decomposition and synthesis – Morphological methods – Axiomatic design. Concept Selection and Testing: Development process – Choosing a concept – Concept screening and scoring – Decision making and evaluation – Methods for testing product concepts.

UNIT-III EMBODIMENT AND DETAIL DESIGN

Product Teardown, Specifications, Portfolios and Architecture: Teardown process, methods and applications – Post teardown report – Benchmarking approach and support tools for benchmarking process – Product portfolios architecture – Architecture type – Platform architecture – Target Specifications – Setting the final specifications – Modularity – Implications of the architecture – Establishing the architecture – Delayed differentiation – Platform planning – Related system-level design. Configuration and Detail Design: Generating, analyzing and evaluating configuration design – Best practices for configuration design – Design for X – Design and manufacturing information – Final design review – Activities beyond detail design. Prototyping: Principles, types and technologies – Understanding prototypes and planning.



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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV DESIGN FOR ENVIRONMENT, MANUFACTURING AND SAFETY

Design for Manufacture and Environment: Cross-functional team – Overview of DFM process – Life cycles – Environmental impacts – Design for environment process. Design for Risk, Reliability and Safety: Classification of societal hazards – Standards – Risk assessment – Design for reliability – Causes of unreliability – Minimizing failure – FMEA – Fault tree analysis – Defects and failure modes – Potential dangers – Guidelines for design for safety – Warning labels.

UNIT-V INDUSTRIAL DESIGN AND PRODUCT DEVELOPMENT ECONOMICS

Industrial Design: Need – Impact – Industrial design process – Management of the industrial design process – Assessing the quality of industrial design. Robust Design: Robust design process. Intellectual Property: Disclosure – Process of pursuing a patent. Product Development Economics: Elements of economic analysis and process. Managing Projects: Understanding and representing tasks – Baseline project planning – Accelerating projects – Project execution – Postmortem project evaluation – Project Portfolio Management (PPM) – Earned Value Management (EVM) – Sustainability and ESG in Project Management.

TEXT BOOKS:

1. Product Design and Development, Karl T Ulrich, Steven D Eppinger and Maria C. Yang, 7/e, 2020, McGraw-Hill Education Pvt.Ltd. Noida.
2. Engineering Design, George E. Dieter and Linda C. Schmidt, 4/e, 2013, McGraw-Hill Education Pvt. Ltd., Noida.

REFERENCE BOOKS:

1. Product Design, Kevin Otto and Kristin Wood, 1/e, 2003, Pearson Education, India.
2. Product Development, Anil Mital, Anoop Desai, Anand Subramanian and Aashi Mital, 1/e, 2007, Butterworth-Heinemann, Elsevier.
3. Integrated Product and Process Design and Development: the Product Realization Process (Special Indian Edition), Edward B. Magrab, Satyandra K. Gupta, F. Patrick McCluskey and Peter A. Sandborn, 2/e, 2010, CRC Press, Taylor & Francis Group, LLC.
4. Product Design for Engineers, Devdas Shetty, 1/e, 2016, Cengage Learning, India.
5. Introduction to Product Design and Development for Engineers, Ali Jamnia, 2018, CRC Press, Taylor & Francis Group, LLC.

COURSE OUTCOMES:

1. Understand To know the design concepts, product development planning and customer requirements
2. Generate the concept using creative problem solving methods, concept generation and testing
3. Realize Product Teardown, Specifications, Portfolios and Architecture, configurations and prototyping
4. Demonstrate and classify The Design aspects for Risk, Reliability and Safety and environments
5. Do industrial design, understand intellectual property, robust design and product development economics

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

**(25D99301A) ADVANCED NUMERICAL METHODS AND
COMPUTATIONAL MATHEMATICS (OE-I)**

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. An ability to independently carry out research/investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program; the mastery should be at a level higher than the requirements of the bachelor program.

UNIT-I NUMERICAL LINEAR ALGEBRA

- Floating-point arithmetic, conditioning, stability, backward/forward error.
- Direct solvers: LU/Cholesky/QR; pivoting and orthogonality.
- SVD, low-rank approximations, pseudoinverses.
- Iterative solvers: Jacobi/Gauss-Seidel/CG/GMRES; basic preconditioning.
- Sparse matrix formats and operations for large-scale systems.
- Krylov subspace and Arnoldi/Lanczos overviews.

UNIT-II DISCRETIZATION OF LINEAR AND NONLINEAR ODES

- Numerical solutions of initial value problems: (single step and multi -step methods)
- Stability of the numerical methods for initial value problems.
- Boundary value problems; shooting method.
- Finite difference for BVP (second and higher order methods), for linear and nonlinear problems
- Consistency-stability-convergence

UNIT-III DISCRETIZATION OF LINEAR AND NONLINEAR PDES

- Finite difference methods for parabolic problems explicit and implicit methods,
- Finite difference for hyperbolic explicit and implicit methods
- Elliptic PDE.
- Consistency, Stability and convergence.
- Lax equivalence and CFL (Courant-Friedrichs-Lewy) ideas.
- Iterative solvers and multigrid overview for discretized systems

UNIT-IV NUMERICAL OPTIMIZATION AND INVERSE PROBLEMS

- Unconstrained methods: gradient, Newton, quasi-Newton, trust-region.
- Constrained methods: KKT conditions, interior-point, SQP principles.
- Nonlinear least squares: Gauss-Newton and Levenberg-Marquardt.
- Regularization (Tikhonov/L1) and model selection concepts.
- Scientific Python stack: `scipy.optimize.minimize`, `scipy.optimize.linprog`, and `scipy.optimize.curve_fit`; solver choice and diagnostics.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V HIGH-PERFORMANCE SCIENTIFIC COMPUTING

- Parallel paradigms: data/task parallelism; domain decomposition fundamentals.
- GPU programming model: threads/warps/memory hierarchy; CUDA libraries.
- MPI and PETSc for scalable sparse linear algebra and time-steppers.
- Performance engineering: profiling, locality, and roofline-style thinking.
- Python at scale: NumPy/SciPy sparse and vectorization; brief Numba/CuPy

TEXT BOOKS:

1. Trefethen, L. N., and D. Bau III, Numerical Linear Algebra, Twenty-Fifth Anniversary Edition, SIAM, 2023.
2. LeVeque, R. J., Finite Difference Methods for Ordinary and Partial Differential Equations: Steady-State and Time-Dependent Problems, SIAM, 2007.
3. Nocedal, J., and S. J. Wright, Numerical Optimization, 2nd ed., Springer, 2006.

REFERENCE BOOKS:

1. Hwu, W.-M. W., and D. B. Kirk, Programming Massively Parallel Processors: A Hands-on Approach, 4th ed., Elsevier, 2022.
2. B. N. dutta, —Numerical linera algebra and Application, - Springer Publications
3. SciPy Project. —Optimization (scipy.optimize) — SciPy Manual|| and —Optimization and Root Finding — SciPy 1.16.2 (stable) Reference.||
4. Balay, S., et al. PETSc/TAO User's Manual. Argonne National Laboratory, ANL-21/39 Rev 3.18release documentation.
5. Logg, A., K.-A. Mardal, and G. N. Wells (eds.). Automated Solution of Differential Equations by the Finite Element Method: The FEniCS Book. Berlin: Springer, 2012.
6. David Kincaid Ward Chenery, — Numerical analysis Mathematics of scientific computing, - AMS Book publishers.
7. M. K. Jain, S. R. K. Iyengar and R. K. Jain, — Computational Methods for Partial Differential Equations, - New Age publications

COURSE OUTCOMES:

1. Analyze conditioning, stability, and error behavior of numerical linear algebra routines for dense and sparse problems (L3, L4).
2. Derive and apply finite difference for BVP for linear and nonlinear models (L3, L4, L5).
3. Derive and apply finite difference for PDE models; assess consistency and stability with Lax equivalence and CFL ideas (L3, L4).

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D99301B) MATHEMATICS FOR MACHINE LEARNING AND DATA SCIENCE (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Equip students with rigorous linear algebra, optimization, and probabilistic tools that underpin modern ML and data science across engineering domains.
2. Enable cross-disciplinary modeling, inference, and decision-making using mathematically principled methods and uncertainty quantification.
3. Develop capability to analyze, formulate, and validate algorithms with provable properties and computational efficiency for real-world applications.

UNIT-I LINEAR ALGEBRA FOUNDATIONS

- o Vector spaces, norms, inner products, orthogonality, and projections
- o Eigenvalues/eigenvectors, spectral theorem, and invariant subspaces
- o Singular value decomposition, low-rank approximations, and Eckart–Young
- o Matrix calculus for ML; gradients/Jacobians/Hessians in matrix form
- o Numerical linear algebra: conditioning, stability, power/QR methods
- o Feature whitening and centering; PCA link to covariance eigen structure

UNIT-II OPTIMIZATION FOR LEARNING

- o Unconstrained methods: gradient descent, line search, Newton/quasi-Newton
- o Constrained optimization: Lagrange multipliers, projected and barrier methods
- o Convex sets/functions, KKT conditions for nonlinear programming problems.
- o Regularization: l_1/l_2 penalties, bias–variance trade-offs in risk minimization
- o Convergence rates and step-size strategies in deterministic models.

UNIT-III PROBABILITY AND STATISTICAL LEARNING

- o Random variables, expectations, covariance; exponential family basics
- o Bayesian inference: conjugacy, MAP vs. MLE, posterior predictive analysis
- o Hypothesis testing and confidence intervals for model comparison
- o Information measures: entropy, KL divergence, mutual information in learning
- o Generalization, overfitting, and model selection criteria(e.g., AIC/BIC/VC-style capacity).

UNIT-IV MODELS AND ALGORITHMS

- o Linear and kernel methods: least squares, logistic regression, and SVMs
- o Dimensionality reduction: PCA, kernel PCA, and manifold intuition
- o Probabilistic models: Naive Bayes, Gaussian mixtures, EM overview
- o Neural network mathematics: backpropagation, initialization, normalization
- o Regularization schemes: weight decay, early stopping, dropout perspectives



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V INTEGRATIVE APPLICATIONS AND WORKED EXAMPLES

- o End-to-end ML pipelines: preprocessing, scaling/whitening, and feature engineering
- o PCA-based exploration and anomaly detection in high-dimensional data
- o SVMs and convex models for fault diagnosis and predictive maintenance
- o Bayesian A/B testing and decision-making under uncertainty
- o Neural network design trade-offs: capacity, optimization, and generalization
- o Model evaluation: calibration, ROC/PR analysis, and uncertainty reporting

TEXT BOOKS:

1. Deisenroth, M. P., Faisal, A. A., & Ong, C. S. Mathematics for Machine Learning. Cambridge University Press, 2020
2. Murphy, K. P. Probabilistic Machine Learning: An Introduction. MIT Press, 2022
3. Boyd, S., & Vandenberghe, L. Convex Optimization. Cambridge University Press, 2004

REFERENCE BOOKS:

1. Goodfellow, I., Bengio, Y., & Courville, A. Deep Learning. MIT Press, 2016
2. Shalev-Shwartz, S., & Ben-David, S. Understanding Machine Learning: From Theory to Algorithms. Cambridge University Press, 2014 3
3. Jolliffe, I. T., & Cadima, J. Principal component analysis: a review and recent developments. Phil. Trans. R. Soc. A, 2016
4. Cover, T. M., & Thomas, J. A. Elements of Information Theory, 2nd ed. Wiley, 2006
5. Murphy, K. P. Probabilistic Machine Learning: Advanced Topics. MIT Press, 2023.

COURSE OUTCOMES:

1. Ability to independently carry out research/investigation and development work to solve practical problems
2. Ability to write and present a substantial technical report/document
3. Demonstrate mastery in the program specialization at a level higher than the bachelor's program requirements
4. Analyze linear models and matrix factorizations for dimensionality reduction and feature representation (L3, L4)
5. Formulate and solve convex and constrained optimization problems; compare first- and second-order methods (L4, L5)
6. Apply probabilistic modeling, Bayesian inference, and information-theoretic measures to estimation and generalization (L3, L4, L5)

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

**(25D99301C) STATISTICAL LEARNING THEORY AND
MATHEMATICAL FOUNDATIONS OF AI (OE-I)**

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. Build rigorous probabilistic, information-theoretic, and optimization foundations that support modern AI across engineering domains.
2. Unify theory and algorithms to enable principled design and analysis of learning systems for cross-disciplinary problems.
3. Connect generalization theory with practice through concise formulations and proofs suited to PG research contexts.

UNIT-I PROBABILITY AND MEASURE FOUNDATIONS

- Probability spaces, σ -algebras, random variables; expectation and conditional expectation.
- Inequalities and concentration: Markov, Chebyshev, Hoeffding; LLN and CLT.
- Modes of convergence and Borel–Cantelli; almost sure vs in- probability convergence.
- Random processes and martingale basics; optional stopping; Doob’s inequality (overview).
- Markov chains: ergodicity, mixing, stationary distributions for modeling sequences

UNIT-II STATISTICAL LEARNING THEORY

- PAC learning model, realizable/agnostic cases; sample complexity and no- free- lunch.
- VC dimension, shattering, Sauer’s lemma; uniform convergence guarantees.
- Empirical risk minimization and structural risk minimization; capacity control.
- Rademacher/Gaussian complexities and symmetrization for data- dependent bounds.
- Algorithmic stability and generalization; regularization and early stopping as capacity control.
- PAC- Bayes bounds and posterior- based generalization certificates.

UNIT-III OPTIMIZATION FOR LEARNING

- Convex analysis: Lipschitzness, smoothness, strong convexity; implications for rates.
- Gradient, stochastic, and variance- reduced methods; step- size and convergence trade-offs.
- Proximal methods and projected gradients; sparsity via ℓ_1 (Lasso) and shrinkage via ℓ_2 (ridge).
- Duality and KKT conditions; constrained learning formulations.
- Nonconvex landscapes in deep networks—saddle points, over-parameterization, and implicit regularization.
- Generalization–optimization interplay: implicit bias of optimizers.



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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV KERNEL AND PROBABILISTIC MODELS

- Reproducing kernel Hilbert spaces, kernel trick, representer theorem.
- Large- margin methods: SVMs, soft margins, hinge loss; primal–dual views.
- Gaussian processes: kernels as priors; posterior prediction and uncertainty quantification.
- Graphical models—Bayesian networks and Markov/conditional random fields for structured prediction; exact inference (variable elimination, junction tree) and approximate methods (loopy belief propagation, variational).
- Hidden Markov models; EM for latent- variable learning.
- Variational inference and message passing for scalable probabilistic AI.

UNIT-V DEEP LEARNING AND INFORMATION THEORY

- Backpropagation (chain rule), initialization, normalization, and activation design.
- Loss functions and calibration; cross- entropy, margin losses, and robust objectives.
- Generalization in deep nets: margins, flat minima, compression, and stability views.
- Information- theoretic tools: entropy, mutual information, KL divergence.
- Information bottleneck and representation learning, with links to PAC- Bayes.
- Worked examples: applying theory to vision, language, and control tasks in engineering.

TEXT BOOKS:

1. Shalev- Shwartz, S., Ben- David, S., Understanding Machine Learning: From Theory to Algorithms, Cambridge University Press, first edition, 2014.
2. Goodfellow, I., Bengio, Y., Courville, A., Deep Learning, MIT Press, 2016.
3. Bishop, C. M., Pattern Recognition and Machine Learning, Springer, 2006.

REFERENCE BOOKS:

1. Vapnik, V. N., The Nature of Statistical Learning Theory, Springer, 1995/1998.
2. Cover, T. M., Thomas, J. A., Elements of Information Theory, 2nd ed., Wiley, 2006.
3. Mohri, M., Rostamizadeh, A., Talwalkar, A., Foundations of Machine Learning, 2nd ed., MIT Press, 2018.
4. Schölkopf, B., Smola, A. J., Learning with Kernels: Support Vector Machines, Regularization, Optimization, and Beyond, MIT Press, 2002.
5. Rasmussen, C. E., Williams, C. K. I., Gaussian Processes for Machine Learning, MIT Press, 2006.

COURSE OUTCOMES:

1. An ability to independently carry out research/investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program; the mastery should be at a level higher than the requirements in the appropriate bachelor program.
4. Analyze probabilistic models, convergence theorems, and stochastic processes underlying learning algorithms (L3, L4).
5. Formulate and prove generalization bounds using VC dimension, Rademacher complexity, and stability (L4, L5).
6. Derive and optimize loss/regularization for linear, kernel, and deep models; justify selections by convexity and smoothness properties (L4, L5).

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D99301D) CHEMISTRY OF NANOMATERIALS AND APPLICATIONS IN ENGINEERING (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:**UNIT-I BASICS OF NANOMATERIALS**

Introduction, Scope of nanoscience and nanotechnology, nanoscience in nature, classification of nanostructured materials, importance of nanomaterials.

UNIT-II SYNTHESIS OF NANOMATERIALS

Top-Down approach, Inert gas condensation, arc discharge method, aerosol synthesis, plasma arc technique, ion sputtering, laser ablation, laser pyrolysis, and chemical vapor deposition method, electrode position method, high-energy ball milling method. Synthetic Methods: Bottom-Up approach, Sol-gel synthesis, microemulsions or reverse micelles, co precipitation method, solvothermal synthesis, hydrothermal synthesis, microwave heating synthesis and sonochemical synthesis.

UNIT-III TECHNIQUES FOR CHARACTERIZATION

Diffraction techniques, spectroscopy techniques, electron microscopy techniques for the characterization of nanomaterials, BET method for surface area analysis, dynamic light scattering for particle size determination.

UNIT-IV DIFFRACTION TECHNIQUES, SPECTROSCOPY TECHNIQUES, ELECTRON MICROSCOPY TECHNIQUES FOR THE CHARACTERIZATION OF NANOMATERIALS, BET METHOD FOR SURFACE AREA ANALYSIS, DYNAMIC LIGHT SCATTERING FOR PARTICLE SIZE DETERMINATION.

Synthesis, properties and applications of the following nanomaterials: fullerenes, carbon nanotubes, 2D-nanomaterial (Graphene), core-shell, magnetic nanoparticles, thermoelectric materials, non-linear optical materials.

UNIT-V ADVANCED ENGINEERING APPLICATIONS OF NANOMATERIALS

Applications of nanoparticles, nanorods, nano wires in Water treatment, sensors, electronic devices, medical domain, civil engineering, chemical engineering, metallurgy and mechanical engineering, food science, agriculture, pollutants degradation.

TEXT BOOKS:

1. NANO: The Essentials: T Pradeep, McGraw-Hill, 2007.
2. Textbook of Nanoscience and nanotechnology: B S Murty, P Shankar, Baldev Rai, BB Rath and James Murday, Univ. Press, 2012.

REFERENCE BOOKS:

1. Concepts of Nano chemistry; Ludovico Cademrtiri and Geoffrey A. Ozin & Geoffrey A. Ozin, Wiley-VCH, 2011.
2. Nanostructures & Nanomaterials; Synthesis, Properties & Applications: Guozhong Cao, Imperial College Press, 2007
3. Nanomaterials Chemistry, C.N.R.Rao, Achim Muller, K.Cheetham, Wiley-VCH, 2007.

COURSE OUTCOMES:

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. III Sem.

L	T	P	C
3	0	0	3

(25D99301E) PHOTONICS FOR ENGINEERS (OE-I)

Course Category	Open Elective (OE)
Course Enrichment Relevance	Employability

COURSE OBJECTIVES:

1. To understand the basic nature and behaviour of light and its propagation in optical media and fibers.
2. To introduce the principles of absorption and emission in optical materials, and to understand the operation of semiconductor light sources and photo detectors..
3. To provide an understanding of nonlinear optical phenomena and the principles of electro-optic, magneto-optic, and acousto-optic modulation used in modern optical devices.
4. To introduce optical fiber characteristics and outline the components and technologies used in modern fiber-optic communication systems.
5. To familiarize students with advanced photonic technologies, including sensors, quantum photonics, plasmonics, metamaterials, and ultrafast/THz systems.

UNIT-I FUNDAMENTALS OF PHOTONICS

Nature of light: wave-particle duality, polarization, coherence. Maxwell's equations and wave propagation in dielectric media. Reflection, refraction, (vector notation) interference, diffraction, dispersion and birefringence

UNIT-II PHOTONIC DEVICES AND COMPONENTS – I

Absorption, spontaneous and stimulated emission. Einstein coefficients, population inversion, optical gain. Semiconductor light sources: LEDs, laser diodes, quantum well lasers. Photodetectors: PIN, avalanche photodiodes, photomultiplier tubes.

UNIT-III PHOTONIC DEVICES AND COMPONENTS – II

Nonlinear optical effects – second-harmonic generation, Kerr effect, four-wave mixing. Electro-optic Magneto optic and acousto-optic modulation principles. Optical modulators and switches (Mach Zehnder Interferometer).

UNIT-IV OPTICAL WAVEGUIDES AND APPLICATIONS

Optical fibers – numerical aperture, V-number, modes, attenuation, dispersion. Fiber-optic communication systems: transmitters, receivers, multiplexing (WDM), optical couplers, ring resonators.

UNIT-V PHOTONIC SYSTEMS AND APPLICATIONS

Photonic sensors – interferometric, fiber Bragg gratings, biosensing. Optical signal processing and computing. Introduction to quantum photonics: single-photon sources, entanglement, and photonic qubits. Plasmonics and metamaterials, Ultrafast and terahertz photonics.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. B.E.A. Saleh & M.C. Teich — Fundamentals of Photonics (Wiley)
2. J. Singh — Semiconductor Optoelectronics: Physics and Technology
3. A. Yariv & P. Yeh — Photonics: Optical Electronics in Modern Communications
4. G. Keiser — Optical Fiber Communications

REFERENCE BOOKS:

1. J. Wilson & J.F.B. Hawkes — Optoelectronics: An Introduction
2. R.W. Boyd — Nonlinear Optics
3. Electromagnetic waves and radiating systems ----- E. Jordan

COURSE OUTCOMES:

1. gain the ability to describe how light behaves and propagates in optical media.
2. explain light-matter interaction mechanisms and analyze the working, characteristics, and applications of LEDs, laser diodes, quantum well lasers and various photodetectors
3. explain key nonlinear effects and analyze the operation of optical modulators and switches such as the Mach-Zehnder Interferometer.
4. Analyze fiber parameters and explain the functioning of transmitters, receivers, WDM systems, couplers and resonator-based communication devices.
5. describe the working of photonic sensors and emerging quantum and ultrafast photonic technologies used in sensing, computation and communication.



SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

**M. Tech (VLSISD Branch)
IV-Semester
Course Structure & Syllabus**

**SANTHIRAM ENGINEERING COLLEGE****(AUTONOMOUS)****DEPARTMENT OF ECE - VLSI SYSTEM DESIGN**

M.Tech. IV Sem. - Course Structure

S. No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				L	T	PI	C	IM	EM	Total
1	25D57401	PR	DISSERTATION PHASE-II	0	0	32	16	100	100	200



SANTHIRAM ENGINEERING COLLEGE, NANDYAL (AUTONOMOUS)

VISION

- ✦ To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

MISSION

- M1:** To provide Advanced Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization by arising a self-sustained University.
- M2:** To establish postgraduate programs in the current and Advanced Technologies.
- M3:** To establish an R&D Consultancy through developing Industry Institute Interaction, building up exceptional infrastructure.
- M4:** To propel every individual, realize and act for the technical development of the society

MOTTO

- ✦ Education for Peace and Progress



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