SANTHIRAM ENGINEERING COLLEGE
(AUTONOMOUS)

Approved by A.I.C.T.E., New Delhi, Permanently Affiliated to JNT University, Ananthapuramu;
Accredited by NAAC with Grade-A, Accredited by NBA (ECE & CSE);
An ISO 9001:2015 Certified Institution, 2(f) & 12(B) recognition by UGC Act, 1956
NH-40, Nandyal-518501, Nandyal (Dist), A.P.

learn-Grow-Empower

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.TECH (ECE-VLSI SD)

REGULAR TWO YEAR PG DEGREE COURSE

(Applicable for the Admitted Batch 2025-26)

REGULATIONS: R-25

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
I-Semester Course Structure

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem. - Course Structure

S.No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				Lecture	Tutorial	Practical	Credits	Internal	External	Total
1	25D57101	PC	CMOS ANALOG IC DESIGN	3	0	0	3	40	60	100
2	25D57102	MC(C)	CMOS DIGITAL IC DESIGN	3	0	0	3	40	60	100
3	25D57103A	PE	CAD FOR VLSI (PE-I)	3	0	0	3	40	60	100
4	25D57103B	PE	MICROCHIP FABRICATION TECHNIQUES (PE-I)	3	0	0	3	40	60	100
5	25D57103C	PE	SCRIPTING LANGUAGES FOR VLSI (PE-I)	3	0	0	3	40	60	100
6	25D57103D	PE	NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)	2	0	0	3	40	60	100
7	25D57103E	PE	MEMS AND NEMS (PE-I)	3	0	0	3	40	60	100
8	25D57104A	PE	ASIC DESIGN (PE-II)	3	0	0	3	40	60	100
9	25D57104B	PE	FPGA ARCHITECTURES AND APPLICATIONS (PE-II)	3	0	0	3	40	60	100
10	25D57104C	PE	DEEP LEARNING FOR VLSI (PE-II)	3	0	0	3	40	60	100
11	25D57104D	PE	DEVICE MODELLING (PE-II)	3	0	0	3	40	60	100
12	25D57104E	PE	MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)	3	0	0	3	40	60	100
13	25D57105	PC	CMOS ANALOG IC DESIGN LAB	0	0	4	2	40	60	100
14	25D57106	PC	CMOS DIGITAL IC DESIGN LAB	0	0	4	2	40	60	100
15	25D57107	MC(C)	RESEARCH METHODOLOGY AND IPR	2	0	0	2	40	60	100
16	25D57108	SC	RTL SYNTHESIS, SIMULATION AND VERIFICATION	0	1	2	2	40	60	100
17	25D57109A	MC(NC)	ENGLISH FOR RESEARCH PAPER WRITING (AC-I)	2	0	0	0	40	0	40
18	25D57109B	MC(NC)	VALUE EDUCATION (AC-I)	2	0	0	0	40	0	40
19	25D57109C	MC(NC)	DISASTER MANAGEMENT (AC-I)	2	0	0	0	40	0	40
20	25D57109D	MC(NC)	ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)	2	0	0	0	40	0	40

R-2025

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
I -Semester Syllabus

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57101) CMOS ANALOG IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

UNIT-I MOS DEVICES AND MODELING

The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling -Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II ANALOG CMOS SUB-CIRCUITS

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage Band gap Reference.

UNIT-III CMOS AMPLIFIERS

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

UNIT-IV CMOS OPERATIONAL AMPLIFIERS

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT-V COMPARATORS

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce.

3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

COURSE OUTCOMES:

1. Understand significance of different biasing styles and apply them for designing analog ICs.
2. Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
3. Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57102) CMOS DIGITAL IC DESIGN

Course Category	**Mandatory Course (credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

UNIT-I MOS DESIGN PSEUDO NMOS LOGIC

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III SEQUENTIAL MOS LOGIC CIRCUITS

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.

COURSE OUTCOMES:

1. Design CMOS inverters with specified noise margins and propagation
2. Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
3. Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
4. Design basic combinational and sequential elements using NMOS and CMOS design strategies.
5. Analyze the dynamic performance of CMOS circuits

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103A) CAD FOR VLSI (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I INTRODUCTION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II PARTITIONING

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing

UNIT-III FLOOR PLANNING

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV PLACEMENT AND ROUTING & GLOBAL ROUTING AND DETAILED ROUTING

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms. Global Routing–Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing–Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing–Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

COURSE OUTCOMES:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement
3. Optimize the implemented design for area, timing and power by applying suitable constraints.
4. Practice the application of fundamentals of VLSI technologies
5. Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103B) MICROCHIP FABRICATION TECHNIQUES (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. Comprehend impact of semiconductor industry on the design of development of integrated circuits.
2. Acquaint with clean room technology
3. Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
4. Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
5. Understand packaging principles

UNIT-I INTRODUCTION TO PROCESSING

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction

UNIT-II PHOTOLITHOGRAPHY

Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT-III DIFFUSION & ION IMPLANTATION

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT-IV FILM DEPOSITIONS AND GROWTH

Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT-V YIELD

Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors. Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

---

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

COURSE OUTCOMES:

1. Understand various stages of fabrication
2. Understand various packaging techniques and Design rules
3. Understand the aspects of diffusion, ion implantation techniques.
4. Classify various thin films and its characteristics.
5. Specify NMOS and CMOS design rules corresponding to package operations.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103C) SCRIPTING LANGUAGES FOR VLSI (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To learn the fundamental syntax, control structures, file I/O, and data processing capabilities of PERL, TCL, and Python.
2. To apply Regular Expressions: Implement regular expressions in scripts to effectively parse and extract specific data from complex EDA tool reports and log files.
3. To automate EDA Tool Flow: Write scripts to control and automate EDA tools, managing workflows for simulation, synthesis, and other design-cycle tasks.
4. To develop VLSI Task Automation: Create efficient automation scripts to handle common VLSI design tasks, such as managing design files, generating reports, and checking for errors.
5. To select Appropriate Tools: Evaluate the requirements of a specific automation task and select the most appropriate scripting language (PERL, TCL, or Python) for the use case.

UNIT-I INTRODUCTION TO SCRIPTING LANGUAGES IN EDA

Introduction to scripting and automation, Scripting vs compiled languages, Using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops – overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

UNIT-II PERL SCRIPTING

Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, Using files and file handles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

UNIT-III TCL SCRIPTING

Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV PYTHON FOR DESIGN AUTOMATION AND DATA PROCESSING

Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, Using os, sys, and subprocess modules, Writing utility scripts for automation

UNIT-V ADVANCED INTEGRATION AND COMPARISON

Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

REFERENCE BOOKS:

1. Robbins, Arnold. Scripting the UNIX System: Using Bash, Perl, and More. Addison-Wesley, 2003. g
2. Ousterhout, John K. Tcl and the Tk Toolkit. 2nd ed., Addison-Wesley Professional, 2009. 3. Python Software Foundation. Python Language Reference Manual. https://docs.python.or

COURSE OUTCOMES:

1. Describe the role of scripting languages in EDA workflows and differentiate between scripting and compiled languages.
2. Write PERL scripts to perform text parsing, data extraction, and report generation.
3. Develop TCL scripts to automate tool commands and control design processes in EDA tools.
4. Construct Python scripts for file handling, data processing, and automation of design-related tasks..
5. Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	3

(25D57103D) NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the basic idea behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and technologies for future applications.
3. To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT-I INTRODUCTION OF NANO MATERIALS AND NANOTECHNOLOGIES

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT-II FUNDAMENTALS OF NANOMATERIALS

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT-III MICRO-AND NANOLITHOGRAPHY TECHNIQUES

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT-IV INTRODUCTION & SYNTHESIS OF CNTS-ARC-DISCHARGE

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V FERROELECTRIC MATERIALS

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application

TEXT BOOKS:

1. Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2ndedition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGrawHill Education 2012.

REFERENCE BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI

COURSE OUTCOMES:

1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To Understand the advantages and Challenges of MEMS
4. To analyze the synthesis of CNTs with applications.
5. To acquire knowledge on the operation and characterization to achieve precisely designed systems

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103E) MEMS AND NEMS (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To introduce Nano-and Microsystems
2. To understand the modeling of micro and nano scale electromechanical systems

UNIT-I INTRODUCTION TO MEMS AND NEMS

MEMS and NEMS definitions, Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Biomimetics, Biological analogies, and design–Biomimetics Fundamentals, Biomimetics for NEMS and MEMS,Nano-ICs and Nano computer architectures

UNIT-II MODELING OF MICRO AND NANO SCALE ELECTROMECHANICAL SYSTEMS

Introduction to modelling, analysis and simulation, basic electro-magnetic with application to MEMS and NEMS, modeling developments of micro-and nano actuators using electromagnetic-Lumped-parameter mathematical models of MEMS, energy conversion in NEMS and MEMS

UNIT-III MEMS FABRICATION TECHNOLOGIES

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation.Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching.

UNIT-IV MICROMACHINING

Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT-V NANOSYSTEMS AND QUANTUM MECHANICS

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TEXT BOOKS:

1. Sergey Edward Lyshevski, Lyshevski Edward Lyshevski, Nano-Electro Mechanical and Micro-Electro Mechanical Systems, Fundamental of Nano-and Micro-Engineering 2005, 2nd Ed., CRC Press.

2. A. S. Edelstein and Cammarata, Nanomaterials: Synthesis, Properties and Applications, 2002, Institute of Physics, Bristol, Philadelphia

REFERENCE BOOKS:

1. Kalantar-ZadehK, Nanotechnology Enabled Sensors, 2008, Springer.
2. Serge Luryi, Jimmy Xu, Alex Zaslavsky, Future trends in MicroElectronics,2007, John Wiley & Sons, Inc. Hoboken, New Jersey

e-Resources and Digital Material:

1. https://onlinecourses.nptel.ac.in/noc22_ee36/preview

COURSE OUTCOMES:

1. Acquire the knowledge of Nano- and Microsystems.
2. Identify the methods of modeling of micro and nano scale electromechanical
3. Ability to design the micro devices, micro systems using the MEMS fabrication process.
4. Gain a knowledge of basic approaches for micromachining
5. Develop experience on micro/nano systems for photonics.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104A) ASIC DESIGN (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand different types of ASICs and their libraries.
2. To understand about programmable ASICs, I/O modules and their interconnects.
3. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT-I INTRODUCTION TO ASICS

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT-II PROGRAMMABLE ASICS AND PROGRAMMABLE ASIC LOGIC CELLS

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT-IV LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT-V SIMULATION, TEST AND ASIC CONSTRUCTION

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

REFERENCE BOOKS:

1. Himanshu Bhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001

COURSE OUTCOMES:

1. Understand different types of ASICs and their libraries.
2. Understand about programmable ASICs, I/O modules and their interconnects.
3. Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.
4. Understand the various Low Level Design Entry and Logic Synthesis
5. Analyze and Simulate the various Tests and ASIC Construction.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104B) FPGA ARCHITECTURES AND APPLICATIONS (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To acquire knowledge about various architectures and device technologies of PLD‟s
2. To comprehend FPGA Architectures
3. To analyze System level Design and their application for Combinational and Sequential Circuits
4. To familiarize with Anti-Fuse Programmed FPGAs
5. To apply knowledge of this subject for various design applications
6. To familiarize with SRAM FPGAs

UNIT-I INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III SRAM PROGRAMMABLE FPGA

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures

UNIT-IV ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT-V DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition

2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning

REFERENCE BOOKS:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

e-Resources and Digital Material:

1. http://www.digimat.in/nptel/courses/video/117108040/L01.html
2. https://www.youtube.com/watch?v=gCAYY0fHPq4

COURSE OUTCOMES:

1. Acquire knowledge about various architectures and device technologies of PLD‟s
2. Comprehend FPGA Architectures
3. Analyze System level Design and their applications for various architectures.
4. Familiarize with Anti-Fuse Programmed FPGAs
5. Apply knowledge of this subject for various design applications.
6. Familiarize with SRAM FPGAs

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104C) DEEP LEARNING FOR VLSI (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To impart knowledge about the Artificial Neural networks and deep learning.
2. To introduce the fundamental concepts relevant to ANN architectures and deep learning algorithms.
3. To understand the applications and use cases of Deep Learning architectures for VLSI circuits and design automation.

UNIT-I INTRODUCTION TO DEEP LEARNING

History and evolution of Deep Learning; Fundamentals of Deep Learning; Training Deep Architectures; Intermediate Representations–Sharing Features and Abstractions across Tasks; Sigmoid Neurons; Gradient Descent; Feedforward Neural Networks; Dropout; Backpropagation – concepts and implementation.

UNIT-II DEEP LEARNING WITH TENSORFLOW

Introduction to Deep Learning and TensorFlow; How Deep Learning Works; Principal Component Analysis (PCA) and its Interpretations; Singular Value Decomposition (SVD); Greedy Layer-wise Pre-training; Improved Activation Functions; Weight Initialization Methods; Batch Normalization; Implementing Basic Deep Learning Models using TensorFlow.

UNIT-III DEEP LEARNING ALGORITHMS AND OPTIMIZATION

Gradient Descent and Backpropagation Techniques; Improving Deep Networks; Multi-Layer Neural Networks; The Challenge of Training Deep Neural Networks; Deep Generative Architectures; Mini-batches and Optimization Techniques; Handling Unstable Gradients; Regularization and Avoiding Over-fitting; Applying Deep Network Theory to Code Implementations.

UNIT-IV ADVANCED DEEP ARCHITECTURES

Introduction to Convolutional Neural Networks (CNNs) for Visual Recognition; Recurrent Neural Networks (RNNs); RNNs in Practice; Long Short-Term Memory (LSTM) and Gated Recurrent Unit (GRU) Architectures; LSTMs and GRUs in Practice; Reinforcement Learning; Importance of Unsupervised Learning; Training Auto encoders.

UNIT-V APPLICATIONS OF DEEP LEARNING IN VLSI

Deep Learning Applications in VLSI Design and Automation – Chip Design, Test Generation, Chip Testing, Diagnosis and Debug, and Characterization; AI-driven Design Flow Automation; Performance Prediction and Optimization in VLSI Circuits using Deep Neural Models.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Deep Learning: Methods and Applications by Li Deng and Dong Yu, now publisher.
2. Neural Networks and Deep Learning by Michael Nielsen, Determination Press.

REFERENCE BOOKS:

1. Hands-On Learning with Scikit-Learn and Tensorflow by Aurelien Geron, Oreilly.
2. Pattern Recognition and Machine Learning by Christopher Bishop, Springer-Verlag Berlin, Heidelberg.
3. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press.

COURSE OUTCOMES:

1. To Describe the key components of AI field and its relation and role in computer science.
2. To Build custom architectures from scratch
3. To be able to apply appropriate architectures for solving, modeling, optimizing and automizing VLSI related options.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104D) DEVICE MODELLING (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the physics of 2-terminal MOS operation and its characteristics
2. To understand the physics of 4-terminal MOSFET operation and its characteristics.
3. To analyze the SOI MOSFET electrical characteristics.

UNIT-I 2-TERMINAL MOS DEVICE

Threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT-II C-V CHARACTERISTICS

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT-III 4-TERMINAL MOSFET

Threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT-IV SUB-THRESHOLD CURRENT MODELS

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT-V SOI MOSFET

Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.

2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009.

COURSE OUTCOMES:

1. Understand the physics of 2-terminal MOS operation and its characteristics
2. Understand the concept of MOS capacitor.
3. Understand the physics of 4-terminal MOSFET operation and its characteristics.
4. To understand Sub threshold current model.
5. Analyze the SOI MOSFET electrical characteristics

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104E) MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To introduce the fundamental principles and operation of semiconductor devices used in analog and digital electronic circuits.
2. To develop the ability to analyze and design basic electronic circuits using diodes, BJTs, and MOSFETs.
3. To explain the characteristics and applications of amplifier and switching circuits in both discrete and integrated forms.
4. To provide understanding of frequency response, feedback, and stability aspects in analog circuit design.
5. To enable students to integrate analog and digital concepts for designing mixed-signal electronic systems

UNIT-I TRANSISTOR FUNDAMENTALS AND BASIC CIRCUIT MODELS

Bipolar Junction Transistor; Physical Structure and Modes of operation, Operation in Active Mode, circuit symbols and conventions, BJT as an Amplifier, small circuit model, BJT as a switch and Ebers Moll Model, Simple BJT inverter and Second Order Effects. MOS Transistor Basic, MOS Parasitic & SPICE Model; CMOS Inverter Basics-I

UNIT-II MOS AND BJT AMPLIFIER DESIGN

Power Analysis SPICE Simulation-I**,** Biasing of MOS Amplifier and its behavior as an analog switch, CMOS CS/CG/SF Amplifier Configuration, Internal cap models and high frequency modelling, JFET, structure and operation. Multistage and Differential Amplifier, Small Signal Operation and Differential Amplifier, MOS Differential Amplier, BiCMOS Amplifier with Active Load, Multistage Amplifier with SPICE Simulation

UNIT-III FREQUENCY RESPONSE AND FEEDBACK IN AMPLIFIERS

S-domain analysis, transfer function, poles and zeros, High Frequency Response of CS and CE Amplifier, Frequency Response of CC and SF Configuration, Frequency Response of the Differential Amplifier, Cascode Connection and its Operation. General Feedback structure and properties of negative feedback, Basic Feedback Topologies, Design of Feedback Amplifier for all configuration, Stability and Amplifier poles, Bode Plots and Frequency Compensation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV OPERATIONAL AMPLIFIERS AND ANALOG FILTERS

Ideal Operational Amplifier and its terminals, Inverting and Non- Inverting Configuration, As an integrator and Differentiator, Introduction to Analog Computer, Large Signal Operation of Op-Amp and Second order offsets. Butterworth and Chebyshev Filters, First and Second Order Filter Functions, Switched Capacitor based filters, Single-Amplifier Biquadratic Filters, Second Order LCR Resonator.

UNIT-V DIGITAL LOGIC AND SEQUENTIAL CIRCUIT DESIGN

Combinational Logic Design, Sequential Logic Design, Clock Strategies for Sequential Design, Concept of Memory & its Designing

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009.

COURSE OUTCOMES:

1. Explain the working principles of semiconductor devices and their roles in electronic circuits.
2. Analyze the performance of analog and digital circuits using appropriate circuit theorems and models.
3. Design and implement amplifier, oscillator, and switching circuits meeting specified requirements.
4. Evaluate the effects of feedback, frequency response, and biasing on circuit stability and performance.
5. Apply learned concepts to design and simulate discrete and integrated circuits used in practical electronic systems.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
0	0	4	2

(25D57105) CMOS ANALOG IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. To explain the Physical Verification in Layout Design
4. To fully appreciate the design and analyze of analog and mixed signal simulation
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments

1. MOS Device Characterization and parametric analysis

2. Common Source Amplifier

3. Common Source Amplifier with source degeneration

4. Cascode amplifier

5. Simple current mirror

6. Cascode current mirror.

7. Wilson current mirror.

8. Differential Amplifier

9. Operational Amplifier

10. Sample and Hold Circuit

11. Direct-conversion ADC

12. R-2R Ladder Type DAC

The students are required to design and implement any TEN Experiments using CMOS 130nm Technology.

The students are required to implement LAYOUTS of any SIX Experiments using CMOS

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

130nm Technology and Compare the results with Pre-Layout Simulation.

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using VLSI design tool.
2. Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. Explain the Physical Verification in Layout Design
4. Fully appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
0	0	4	2

(25D57106) CMOS DIGITAL IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

1. **Inverter Characteristics.**
2. **NAND and NOR Gate**
3. **XOR and XNOR Gate**
4. **2:1 Multiplexer**
5. **Full Adder**
6. **RS-Latch**
7. **Clock Divider**
8. **JK-Flip Flop**
9. **Synchronous Counter**
10. **Asynchronous Counter**
11. **Static RAM Cell**
12. **Dynamic Logic Circuits**
13. **Linear Feedback Shift Register**

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using any VLSI design tool
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Explain the Physical Verification in Layout Extraction
4. Fully appreciate the design and analyze of CMOS Digital Circuits
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	2

(25D57107) RESEARCH METHODOLOGY AND IPR

Course Category	**Mandatory Course (credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the research design process and data collection methods.
2. To develop skills in data analysis and reporting.
3. To familiarize students with intellectual property rights (IPR) and patents.
4. To apply research skills in real-world contexts.

UNIT-I FUNDAMENTALS OF RESEARCH METHODOLOGY

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

Learning Outcomes

- Recall key concepts of the research process, including different types and approaches to research, and the importance of ethics.
- Differentiate between qualitative and quantitative research approaches and the various uses of secondary data.
- Identify the core principles of research design and ethics, including plagiarism and documentation styles.
- Explain the significance of reasoning and ethical conduct in all stages of the research process.

Apply knowledge of different documentation styles, such as APA and IEEE, to properly cite sources and avoid plagiarism.

UNIT-II DATA COLLECTION AND SOURCES

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

Learning Outcomes

- Identify different types of data and the various methods for collecting both primary and secondary data.
- Explain the importance of data quality and ethical considerations in data collection.
- Differentiate between primary, secondary, and Big Data sources.
- Describe the various tools and technologies used for effective data collection.

Analyze the ethical implications of data collection and ensure data quality in a research study.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-III DATA ANALYSIS AND REPORTING

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

Learning Outcomes

- Apply knowledge of multivariate analysis and experimental research to develop hypotheses and analyze data.
- Explain the process of measurement systems analysis and error propagation in experimental design.
- Formulate clear and concise abstracts, introductions, and methodologies for research papers.
- Write effective results and discussion sections based on data analysis.

Develop comprehensive research papers and proposals based on proper data analysis and reporting guidelines.

UNIT-IV UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Learning Outcomes

- Recall the fundamental concepts of Intellectual Property (IP) and its evolution.
- Describe the roles of organizations like **WIPO** and **WTO** in the establishment of IPR.
- Differentiate between various types of IPR, including trade secrets and trademarks.
- Explain the common rules and features of IPR agreements and the role of UNESCO.

Analyze the relationship between IPR and biodiversity, and its broader impact.

UNIT-V PATENTS

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Learning Outcomes

- Explain the objectives, benefits, and key features of a patent, including the concept of an inventive step.
- Differentiate between the various types of patent applications and the e-filing process.
- Describe the process of patent examination, grant, and revocation.
- Identify the roles of patent agents and the process for their registration.

Analyze the concepts of equitable assignments, licenses, and licensing of related patents.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004

2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

REFERENCE BOOKS:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.
6. Peter Elbow, Writing With Power, Oxford University Press, 1998.

e-Resources and Digital Material:

1. Coursera / edX – Research Methodology and Data Analysis courses
2. Springer Link & ScienceDirect – Latest journals on research design and statistics
3. Google Scholar – Free access to research papers
4. NCBI Bookshelf – Open-access research methodology resources
5. Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

COURSE OUTCOMES:

1. Recall key concepts and terminology related to research design, data collection, and intellectual property rights.
2. Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.
3. Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.
4. Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.
5. Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods. 6. Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
0	1	2	2

(25D57108) RTL SYNTHESIS, SIMULATION AND VERIFICATION

Course Category	**Skill Oriented Course (SC)**
Course Enrichment Relevance	**Skill Development**

COURSE OBJECTIVES:

1. The simulation of combinational and sequential circuits.
2. FSM based designs.
3. Implementation of DFT and FFTs.
4. Verify layout of basic digital circuits.

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (SystemVerilog/VHDL basics).
- Lab:

1. Write synthesizable Verilog/SystemVerilog code for:

   a) Half Adder, Full Adder

   b) 4-bit Ripple Carry Adder

   c) 4-bit Synchronous Counter (Up/Down)

2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:

1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool

2. Generate gate-level netlist and analyze area, delay, power reports.

3. Apply constraints (clock, timing) and observe impact on synthesis

results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations

1. Develop testbenches for:
   a) 4-bit ALU (add, sub, AND, OR).
   b) Universal Shift Register.
2. Perform functional simulation using EDA tools
3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.

1. Write self-checking testbenches for combinational and sequential circuits.
2. Use assertion-based verification (SystemVerilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:

1. UART Transmitter/Receiver
2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)

3. FIFO Buffer with full/empty flags

TEXT BOOKS:

1. Samir Palanitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson, 2007.
2. Michael Ciletti – Advanced Digital Design with the Verilog HDL.
3. Chris Spear & Greg Tumbush – SystemVerilog for Verification.
4. David Rich – Design and Verification with SystemVerilog.
5. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.
6. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs.
5. Build and verify various digital circuits.4. Employ simulation and formal verification methodologies, including assertion-based verification and equivalence checking.
6. Integrate RTL modules and perform case-study designs covering hierarchical design, DFT, HLS, and FPGA implementation.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109A) ENGLISH FOR RESEARCH PAPER WRITING (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To equip students with the fundamentals of academic English for research paper writing.
2. To develop students' advanced reading skills for analyzing and evaluating research articles.
3. To refine students' grammar and language skills for clarity and precision in research writing.
4. To master the skills of revising, editing, and proofreading research papers.
5. To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.

UNIT-I FUNDAMENTALS OF ACADEMIC ENGLISH

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT-II READING SKILLS FOR RESEARCHERS

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT-III GRAMMAR REFINEMENT FOR RESEARCH WRITING

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT-IV MASTERY IN REFINING WRITTEN CONTENT/EDITING SKILLS

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V TECHNOLOGY AND LANGUAGE FOR RESEARCH

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

TEXT BOOKS:

1. Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge,2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

REFERENCE BOOKS:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007
3. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005
4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R.Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R.How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

e-Resources and Digital Material:

1. https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/
2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview
3. Writing in the Sciences" – Stanford University (MOOC on Coursera) https://www.coursera.org/learn/sciwrite
4. Academic Phrasebank – University of Manchester http://www.phrasebank.manchester.ac.uk
5. OWL (Online Writing Lab) – Purdue University, https://owl.purdue.edu *(Resources on APA/MLA formats, grammar, structure, paraphrasing)*
6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources

COURSE OUTCOMES:

1. Recall the key language aspects and structural elements of academic writing in research papers.
2. Explain the importance of clarity, precision, and objectivity in research writing.
3. Apply critical reading strategies and advanced grammar skills to analyze and write research papers.

4. Analyze research articles and identify the strengths and limitations of different methodologies.
5. Evaluate research papers to check for plagiarism, structure, clarity, and language accuracy.
6. Evaluate the effectiveness of different language and technology tools in research writing, including AI-assisted tools and plagiarism detection software and Develop a well-structured research paper that effectively communicates complex ideas.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109B) VALUE EDUCATION (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

UNIT-I VALUES AND SELF-DEVELOPMENT

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II IMPORTANCE OF VALUES

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III PERSONALITY AND BEHAVIOR DEVELOPMENT

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV AVOID FAULT THINKING

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V CHARACTER AND COMPETENCE

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

COURSE OUTCOMES:

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109C) DISASTER MANAGEMENT (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Environment & Sustainability**

COURSE OBJECTIVES:

1. To enable the students to understand the fundamental concepts of disasters, hazards, their factors, and significance with special reference to India.
2. To prepare them to classify and analyze different types of natural and man-made disasters, their causes, magnitude, and impacts.
3. To foster them develop understanding of disaster preparedness, monitoring systems, and the role of government, community, and media.
4. To equip them in learning risk assessment techniques, disaster risk reduction strategies, and the importance of global and national cooperation. 5. To foster their ability to think critically and respond to disasters and design effective mitigation measures (structural and non-structural) with a focus on emerging trends and Indian disaster management programs.

UNIT-I INTRODUCTION & DISASTER PRONE AREAS IN INDIA

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude. Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT-II REPERCUSSIONS OF DISASTERS AND HAZARDS

Economic Damage - Loss of Human and Animal Life - Destruction of Ecosystem - Natural Disasters - Earthquakes, Volcanism, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster - Nuclear Reactor Meltdown - Industrial Accidents - Oil Slick sand Spills - Outbreaks of Disease and Epidemics War and Conflicts

UNIT-III DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness - Monitoring of Phenomena - Triggering a Disasteror Hazard - Evaluation of Risk-Application of Remote Sensing - Data from Meteorological and Other Agencies - Media Reports- Governmental and Community Preparedness

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV RISK ASSESSMENT DISASTER RISK

Disaster Risk -Concept and Elements, Disaster Risk Reduction - Global and National Disaster Risk Situation -Techniques of Risk Assessment – Global Co-Operation in Risk Assessment and Warning - People's participation in Risk Assessment – Strategies for Survival

UNIT-V DISASTER MITIGATION

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS:

1. Gupta, H. K. Disaster Management. Universities Press, 2003
2. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.

REFERENCE BOOKS:

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.
4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.
5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

e-Resources and Digital Material:

1. National Disaster Management Authority (NDMA), India: https://ndma.gov.in – official guidelines, reports, and policy frameworks.
2. United Nations Office for Disaster Risk Reduction (UNDRR): https://www.undrr.org – Sendai Framework, global risk reduction strategies.
3. Global Disaster Alert and Coordination System (GDACS): https://www.gdacs.org – real-time disaster alerts.
4. World Health Organization (WHO) – https://www.who.int/emergencies – disaster-related health guidelines.

COURSE OUTCOMES:

1. Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.

2. Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters.
3. Assess the economic, social, and ecological repercussions of major natural and man-made disasters.
4. Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.
5. Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.
6. Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109D) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

1. To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.
2. To make them understand the need for protecting traditional knowledge and its significance in the global economy.
3. To make them understand the legal frame work and policies related to traditional knowledge protection.
4. To enable them to understand the relationship between traditional knowledge and intellectual property rights.
5. To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

UNIT-I INTRODUCTION TO TRADITIONAL KNOWLEDGE

Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge - Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge.

UNIT-II PROTECTION, NEED, SIGNIFICANCE, VALUE AND ROLE OF TRADITIONAL KNOWLEDGE

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK

UNIT-III LEGAL FRAME WORK

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV TRADITIONAL KNOWLEDGE AND INTELLECTUAL PROPERTY

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT-V TRADITIONAL KNOWLEDGE IN DIFFERENT SECTORS

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TKTraditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

TEXT BOOKS:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh,Traditional Knowledge System and Technology in India, PratibhaPrakashan 2012.

REFERENCE BOOKS:

1. Pride of India: A Glimpse into India’s Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. “On Astronomy in Ancient India”, Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

e-Resources and Digital Material:

1. https://www.youtube.com/watch?v=LZP1StpYEPM
2. http://nptel.ac.in/courses/121106003/

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Define and explain the concept of traditional knowledge, its nature, characteristics, and scope
2. Understand the need for protecting traditional knowledge and its significance in the global economy
3. Explain the legal framework and policies related to traditional knowledge protection
4. Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology
5. Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change
6. Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms

R-2025

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
II-Semester Course Structure

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem. - Course Structure

S.No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				Lecture	Tutorial	Practical	Credits	Internal	External	Total
1	25D57201	PC	CMOS MIXED SIGNAL IC DESIGN	3	0	0	3	40	60	100
2	25D57202	PC	PHYSICAL DESIGN AUTOMATION	3	0	0	3	40	60	100
3	25D57203A	PE	DIGITAL VLSI TESTING (PE-III)	3	0	0	3	40	60	100
4	25D57203B	PE	INTEGRATED CIRCUITS, MOSFETS, OP-AMPS AND THEIR APPLICATIONS (PE-III)	3	0	0	3	40	60	100
5	25D57203C	PE	SOC TESTING AND VERIFICATION (PE-III)	3	0	0	3	40	60	100
6	25D57203D	PE	SEMICONDUCTOR MEMORY DESIGN AND TESTING (PE-III)	3	0	0	3	40	60	100
7	25D57203E	PE	ADVANCED VLSI INTERCONNECTS (PE-III)	3	0	0	3	40	60	100
8	25D57204A	PE	SEMICONDUCTOR DEVICES FOR NEXT GENERATION FETS: A PHYSICS PERSPECTIVE (PE-IV)	3	0	0	3	40	60	100
9	25D57204B	PE	DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS (PE-IV)	3	0	0	3	40	60	100
10	25D57204C	PE	ALGORITHMS FOR VLSI DESIGN (PE-IV)	3	0	0	3	40	60	100
11	25D57204D	PE	LOW POWER VLSI DESIGN (PE-IV)	3	0	0	2	40	60	100
12	25D57204E	PE	VLSI SIGNAL PROCESSING (PE-IV)	3	0	0	2	40	60	100
13	25D57205	PC	CMOS MIXED SIGNAL IC DESIGN LAB	0	0	4	2	40	60	100
14	25D57206	PC	PHYSICAL DESIGN AUTOMATION LAB	0	0	4	2	40	60	100
15	25D57207	MC(C)	QUANTUM TECHNOLOGIES AND APPLICATIONS	2	0	0	2	40	60	100
16	25D57209A	PE	ENTREPRENEURSHIP ESSENTIALS (AC-II)	2	0	0	0	40	0	40
17	25D57209B	PE	PEDAGOGY STUDIES (AC-II)	2	0	0	0	40	0	40
18	25D57209C	PE	YOGA FOR STRESS MANAGEMENT (AC-II)	2	0	0	0	40	0	40
19	25D57209D	MC(NC)	CONSTITUTION OF INDIA (AC-II)	2	0	0	0	40	0	40

R-2025

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
II -Semester Syllabus

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57201) CMOS MIXED SIGNAL IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To demonstrate first order filter with least interference
2. 2. To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects
3. 3. To design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I UNIT-I

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT-II PHASED LOCK LOOP (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III DATA CONVERTER

Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV A TO D CONVERTERS

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D converters, Time- interleaved converters

UNIT-V OVERSAMPLING CONVERTERS

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

TEXT BOOKS:

1. 1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
   2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010
2. 2. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. 1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. 2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005. 3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009

COURSE OUTCOMES:

1. 1. To understand, analyze and design Switched capacitor filter circuits
2. 2. To analyze and design the PLL circuits
3. 3. To analyze and design the different D/A converters
4. 4. To analyze and design the different A/D converters
5. 5. To analyze modulators, filters and converters.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57202) PHYSICAL DESIGN AUTOMATION

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To understand relation between automation algorithms and constraints posed by VLSI technology
2. 2. To adopt algorithms to meet critical design parameters.
3. 3. To design area efficient logics by employing different routing algorithms and shape functions
4. 4. To simulate and synthesis different combinational and sequential logics

UNIT-I UNIT-I

VLSI Design Automation Tools:

Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT-II UNIT-II

Layout:

Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT-III UNIT-III

Floor Planning and Routing:

Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT-IV UNIT-IV

Simulation and Logic Synthesis:

Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis

UNIT-V UNIT-V

High-Level Synthesis:

Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

TEXT BOOKS:

1. 1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998

2. 2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999

REFERENCE BOOKS:

1. 1. S.M. Sait, H. Youssef, VLSI Physical Design Automation, World scientific, 1999
2. 2. M. Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

COURSE OUTCOMES:

1. 1. To understand the various VLSI design flows and applications in the VLSI technology
2. 2. To remember the design rules and apply in the VLSI design verification process.
3. 3. To understand and apply routing and placement algorithms to meet critical design parameters
4. 4. To evaluate the VLSI design for logical synthesis using simulation tools
5. 5. To apply various synthesis models for the different combinational and sequential circuits.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203A) DIGITAL VLSI TESTING (PE-III)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To introduce the importance of testing in the VLSI design cycle and the challenges associated with modern complex IC designs
2. 2. To explain the fault models, test generation methods, and fault simulation techniques essential for detecting and diagnosing design defects
3. 3. To familiarize students with the principles and architectures of Design for Testability (DFT) for efficient test implementation
4. 4. To develop understanding of built-in self-test (BIST), scan design, and boundary scan architectures for improved test coverage and yield
5. 5. To enable learners to design VLSI systems with testability features ensuring reliability, manufacturability, and cost-effectiveness

UNIT-I FUNDAMENTALS OF VLSI TESTING

Introduction: Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues

UNIT-II DESIGN FOR TESTABILITY (DFT) TECHNIQUES

Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture, Scan design rules, Scan design flow. Fault Simulation: Introduction, Simulation models

UNIT-III FAULT SIMULATION AND TEST GENERATION

Fault Simulation: Logic simulation, Fault simulation. Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms. ATPG for non-stuck-at faults, other issues in test generation Built-In-Self-Test: Introduction, BIST design rules

UNIT-IV BUILT-IN-SELF-TEST (BIST) AND TEST COMPRESSION

Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures. Test Compression: Introduction, Stimulus compression, Response compression.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V MEMORY, POWER, AND THERMAL AWARE TESTING

Memory Testing: Introduction, RAM fault models, RAM test generation. Memory Testing: Memory BIST Power and Thermal Aware Test: Importance, Power models, Low power ATPG. Power and Thermal Aware Test: Low power BIST, Thermal aware techniques

TEXT BOOKS:

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2000
2. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann Publishers, 2006
3. N. K. Jha and S. Gupta, Testing of Digital Systems, Cambridge University Press, 2003.
4. P. K. Lala, Digital Circuit Testing and Testability, Academic Press, 1997
5. B. K. Singh, VLSI Testing and Design for Testability, New Age International Publishers, 2020

REFERENCE BOOKS:

1. 1. Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1994.
2. 2. Charles E. Stroud, A Designer???s Guide to Built-In Self-Test, Springer, 2002.

COURSE OUTCOMES:

1. 1. Explain the role and significance of testing in the VLSI design process and its impact on product yield and quality.
2. 2. Identify and analyze various fault models and apply test generation algorithms to detect faults in digital circuits.
3. 3. Design circuits incorporating DFT techniques such as scan chains, boundary scan, and BIST architectures.
4. 4. Evaluate the effectiveness of different testing strategies in achieving high fault coverage and manufacturability.
5. 5. Apply VLSI testing principles and DFT methodologies to design reliable and testable integrated circuits for large-scale production

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203B) INTEGRATED CIRCUITS, MOSFETS, OP-AMPS AND THEIR APPLICATIONS (PE-III)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To provide fundamental knowledge of IC fabrication processes, MOSFET parameters, and Op-Amp characteristics
2. 2. To enable students to understand the principles of operational amplifiers and their internal circuit architecture
3. 3. To familiarize students with various feedback techniques and types of noise encountered in analog circuits.
4. 4. To develop the ability to design and analyze amplifiers, oscillators, and filters using operational amplifiers
5. 5. To cultivate practical skills in constructing, testing, and troubleshooting analog electronic circuits

UNIT-I FUNDAMENTALS OF INTEGRATED CIRCUIT TECHNOLOGY

Introduction to Integrated Circuit (IC) Technology, Evolution and Importance of ICs, Fabrication Processes for Integrated Circuits, Basic IC Manufacturing Steps: Oxidation, Diffusion, Ion Implantation, Photolithography, Metallization, Overview of Bipolar and MOS Technologies.

UNIT-II OPERATIONAL AMPLIFIERS

Fundamentals and Characteristics:

Introduction to Operational Amplifiers (Op-Amps), Characteristics and Internal Structure of Op-Amps, Common Mode Rejection Ratio (CMRR) and its Importance, Input Offset Voltages, Input Bias, and Offset Currents, Frequency Response of Op-Amps.

UNIT-III MOSFET TECHNOLOGY AND APPLICATIONS

MOSFET Fabrication Techniques and Structure, MOSFET Characteristics and Applications, Current Mirrors using MOSFETs, Design and Analysis of Current Mirror Circuits in Integrated Systems.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV FEEDBACK, AMPLIFIERS, AND SIGNAL PROCESSING CIRCUITS

Frequency Response and Feedback Techniques in ICs, Design and Analysis of Comparators and Instrumentation Amplifiers, Active Filters and their Realizations, Oscillator Design using Op-Amps and MOS Circuits.

UNIT-V DATA CONVERSION AND PRACTICAL OP-AMP APPLICATIONS

Noise in Electronic Circuits, Op-Amp Based Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC) using Op-Amps, Reading and Interpreting Op-Amp Datasheets, Design Considerations and Real-World Applications

TEXT BOOKS:

1. 1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition
2. 2. CMOS Digital Integrated Circuits Analysis and Design ??? Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011

REFERENCE BOOKS:

1. 1. Gray, Hurst, Lewis, and Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, 5th edition, 2009
2. 2. Horowitz and Hill, The Art of Electronics, Cambridge Univ. Press, 1999
3. 3. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001

COURSE OUTCOMES:

1. 1. Understand and analyze the characteristics and operation of operational amplifiers.
2. 2. Demonstrate knowledge of IC fabrication technology and the equipment used in integrated circuit manufacturing.
3. 3. Explain different feedback configurations and identify sources and effects of noise in analog systems
4. 4. Design and analyze various amplifier and oscillator circuits using operational amplifiers.
5. 5. Design, simulate, and troubleshoot analog filters and other practical analog circuits using Op-Amps.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203C) SOC TESTING AND VERIFICATION (PE-III)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To understand the concepts of faults and testing in SoC
2. 2. To implement the faults using simulation tools
3. 3. To analyze BIST systems

UNIT-I INTRODUCTION TO TESTING

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II LOGIC AND FAULT SIMULATION

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT-III TESTABILITY MEASURES

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV BUILT-IN SELF-TEST

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V

Boundary Scan Standard:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

---

1. 1. M.L. Bushnell, V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Pulishers
2. 2. M. Abramovici, M.A.Breuer and A.D Friedman, Digital Systems and Testable Design, Jaico Publishing House.

REFERENCE BOOKS:

1. 1. P.K. Lala, Digital Circuits Testing and Testability, Academic Press

COURSE OUTCOMES:

1. 1. To understand the types faults and the concepts of faults and testing in SoC
2. 2. To understand the algorithms to detect the faults using simulation tools.
3. 3. To understand and apply the concepts of observability and controllability.
4. 4. To apply and evaluate the circuit under test using BIST
5. 5. To apply and evaluate the circuit under test using Boundary Scan tests.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203D) SEMICONDUCTOR MEMORY DESIGN AND TESTING (PE-III)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To understand different types of memories, their architectural and different packing techniques of memories.
2. 2. To build fault models for memory testing
3. 3. To analyze different parameters that lead malfunctioning of memories
4. 4. To design reliable memories with efficient architecture to improve processes times and power.

UNIT-I RANDOM ACCESS MEMORY TECHNOLOGIES

SRAM: SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II NON-VOLATILE MEMORIES

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT-III MEMORY FAULT MODELING TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT-V ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKING TECHNOLOGIES

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. 1. Semiconductor Memories Technology Ashok K. Sharma, 2002, Wiley.
2. 2. Advanced Semiconductor Memories Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley

REFERENCE BOOKS:

1. 1. Modern Semiconductor Devices for Integrated Circuits Chenming C Hu, First Edition. Prentice all

COURSE OUTCOMES:

1. 1. To understand and analyze the SRAM and DRAM cell structures
2. 2. To understand, remember and apply different types of memory cells in suitable applications
3. 3. To analyze and evaluate fault models for memory testing
4. 4. To analyze the memories for reliability and radiation effects
5. 5. To understand and remember advanced manufacturing technologies in memory cell designs.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57203E) ADVANCED VLSI INTERCONNECTS (PE-III)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the fundamentals of VLSI interconnect modeling and delay estimation.
2. To study distributed RC and RLC interconnect models and analyze signal propagation delays.
3. To explore inductive, skin, and electromigration effects influencing interconnect performance.
4. To analyze and mitigate crosstalk and extract key interconnect parameters.
5. To introduce quantum effects in nanoscale and graphene-based interconnects.

UNIT-I INTRODUCTION TO VLSI INTERCONNECTS

Introduction to VLSI Interconnects, the Distributed RC Interconnect Model, Elmore Delay in Interconnects, and Scaling Effects in Interconnects. Simulation and Delay Mitigation Techniques in RC Interconnects

UNIT-II INDUCTIVE EFFECTS IN INTERCONNECTS

Inductive Effects in Interconnects, Distributed RLC Interconnect Model, and Transmission Line Equations. When to Consider Inductive Effects, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, and RLC Interconnect Simulation Techniques.

UNIT-III SKIN EFFECT AND ELECTROMIGRATION

Origin of the Skin Effect and its Impact on Signal Integrity, Effective Resistance at High Frequencies, and Power Dissipation in Interconnects. Electromigration in Interconnects, Physical Mechanisms, Reliability Issues, and Mitigation Techniques for Electromigration.

UNIT-IV CROSSTALK AND PARAMETER EXTRACTION

Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, and Crosstalk Mitigation Techniques. Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance and Inductance, Estimation of Interconnect Parameters from S-Parameters

UNIT-V QUANTUM EFFECTS IN INTERCONNECTS

Quantum Conductance and Quantum Capacitance, Kinetic Inductance, and Graphene Nanoribbon Interconnects. Quantum Effects in Nanoscale Interconnects, Analysis and Simulation of Interconnects Considering Quantum Effects.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Banerjee, K., and Mehrotra, A., Analysis and Optimization of On-Chip Inductive Interconnects, Springer, 2001
2. Bakoglu, H. B., Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley, 1990.

REFERENCE BOOKS:

1. Deutsch, A., et al., High-Speed Signal Propagation: Advanced Black Magic, Prentice Hall, 2003.
2. Rabaey, J. M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall, 2003.
3. Zhang, L., and Joshi, R. V., Interconnect Analysis and Design for Advanced VLSI, Springer, 201

COURSE OUTCOMES:

1. Understand the distributed RC and RLC models for on-chip interconnects.
2. Analyze the delay and signal integrity issues caused by inductive and resistive effects.
3. Identify and mitigate electromigration and skin effect problems in interconnects.
4. Evaluate and simulate crosstalk and extract interconnect parameters effectively.
5. Apply quantum and nanoscale interconnect concepts in advanced VLSI systems

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57204A) SEMICONDUCTOR DEVICES FOR NEXT GENERATION FETS: A PHYSICS PERSPECTIVE (PE-IV)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To introduce the fundamental principles of Metal-Oxide-Semiconductor (MOS) capacitors and their role in the operation of MOS-based devices
2. 2. To provide a comprehensive understanding of various Field-Effect Transistor (FET) architectures, including MOSFETs, FinFETs, GAA FETs, and High-Power FETs
3. 3. To explore the challenges, limitations, and scaling issues in conventional CMOS technology and motivate the need for beyond-CMOS devices
4. 4. To familiarize students with emerging device technologies such as Negative Capacitance FETs (NC-FETs) and 2D material-based transistors for future nano electronic applications
5. 5. To enable learners to analyze device performance parameters and understand their implications for modern VLSI circuit design and fabrication

UNIT-I MOS CAPACITORS AND MOSFET FUNDAMENTALS

MOS Capacitors: Introduction of Metal-Oxide-Semiconductor, Energy Band Diagram of MOS Capacitors, Second Order Effects in MOS Capacitors, C-V of MOS capacitor

MOSFET and Application: Introduction of MOSFET, I-V and C-V Characteristics of MOSFETs, Capacitance Modeling for HF & LF, High and Low Frequency Modeling in Bulk MOSFET, MOSFET as Switch and Amplifier

MOSFET SPICE Models: Introduction to MOSFET SPICE Models, Discuss Various SPICE Models equations, SPICE Models for the MOS Transistor, The SPICE Diode Models, Practical Aspects and Simulation Techniques

UNIT-II ADVANCED MOSFET ARCHITECTURES AND SHORT-CHANNEL EFFECTS

Semiconductor Heterostructures: Introduction, Carriers and Transports, Band Diagram of Heterostructure, PN Heterojunction Diode, Properties and Application

Short Channel Effects: Introduction to 2nd Order Effects at Lower Technology Node, Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), and Subthreshold Swing (SS), Mobility and Scattering Effects, Velocity Saturation Effects, Hot Carrier Effect, Self-heating Effect

Double Gate MOSFET: Introduction to Double Gate MOSFET, SOI MOSFET, Partially and Fully Depleted MOSFET, Subthreshold Swing and Transconductance, Small and Large Signal Modeling, Introduction of Junction less MOSFET

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-III EMERGING TRANSISTOR TECHNOLOGIES

FinFET and GAA FET:

FinFET: A successor of MOSFET, Introduction to FinFETs Structure, Structural Classification of FinFETs, RLC FinFET Modeling, High Frequency Small Signal Modeling, Device Circuit Co-Design using FinFET with Suitable Examples

Gate-All-Around FETs: Sub 5nm Node Devices: Introduction of Different Types of GAA Structure, Current Trends in GAA Devices, Nanosheet FET, Process Variation in Nanosheet FET, Analog Perspective of Nanosheet FET

Forksheet FET and CFET: Sub 3nm Node, Introduction to Forksheet FET, Discuss the challenges of Forksheet, CFET Advancements and Industry Adoption, Discuss the Circuit Design Challenges with CFET, CFET Optimization for Semiconductor Scaling

UNIT-IV BEYOND-CMOS DEVICES AND NOVEL CONCEPTS

Negative Capacitance: Improved Subthreshold Swing: Negative Capacitance (NC): A Concept Note, FeFET & FeFET Based Memory, Advantages and Challenges of NCFETs, Modelling of NCFETs, Introduction of Phase Transition Material (PTM). III-V Semiconductor FETs: Introduction of III-V materials, Materials for High-Speed Devices and Circuits, High Electron Mobility Transistors (HEMT): Modelling and Simulation, III-V Semiconductor FET, Application of III-V material-based FET.

UNIT-V 2D MATERIAL-BASED DEVICES AND FUTURE NANOELECTRONICS

2D Materials for Next Generation Computing: Fundamental Understanding of 2D Material, Physics Properties of 2D Materials, Challenges and Future Scope, Application of 2D Material, 2D-FETs

TEXT BOOKS:

1. 1. Neamen, Donald A. Semiconductor physics and devices: basic principles. New York, NY: McGraw-Hill, 2012.
2. 2. R. F. Pierret, Semiconductor Device Fundamentals, 1996.
3. 3. Jean-Pierre Colinge, FinFETs and Other Multi-Gate Transistors, 2008.

REFERENCE BOOKS:

1. 1. S. M. Sze and M. K. Lee, Semiconductor Devices: Physics and Technology, 3rd Edition, Wiley, 2012.
2. 2. D. Nirmal, J. Ajayan, and P. J. Fay (Editors), Semiconductor Devices and Technologies for Future Ultra Low Power Electronics, CRC Press, 2021.
3. 3. S. Tayal, A. K. Sharma, and A. K. Singh (Editors), Advanced Ultra Low-Power Semiconductor Devices: Design and Applications, Scrivener Publishing, Wiley, 2022.

e-Resources and Digital Material:

1. https://onlinecourses.nptel.ac.in/noc25_ee75/preview

COURSE OUTCOMES:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

---

1. 1. Explain the structure and operation of MOS capacitors and the principles governing charge, capacitance, and threshold behavior
2. 2. Analyze and compare different types of FETs based on their device structures, electrical characteristics, and fabrication techniques
3. 3. Evaluate the technological limitations of CMOS scaling and identify potential solutions through novel device architectures
4. 4. Demonstrate an understanding of next-generation transistor technologies such as NC-FETs, GAA-FETs, and 2D-material-based devices in the context of VLSI evolution.
5. 5. Apply the acquired knowledge to assess device suitability for low-power, high-performance, and high-density VLSI design applications.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57204B) DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS (PE-IV)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

UNIT-I CMOS DEVICE FUNDAMENTALS AND INVERTER CHARACTERISTICS

CMOS transistor fundamentals and current modeling, CMOS inverter structure and voltage transfer characteristics, Noise margins and switching thresholds, Dynamic behavior and delay modeling of CMOS inverters.

UNIT-II DELAY ANALYSIS AND OPTIMIZATION IN CMOS CIRCUITS

RC delay modeling in interconnects and logic paths, Delay estimation using logical effort and Elmore delay, Techniques for delay and performance optimization, Trade-offs among delay, area, and power metrics

UNIT-III LOGIC DESIGN STYLES AND INTERCONNECT MODELING

Overview of CMOS combinational circuit families (static, dynamic, pass-transistor logic), Stick diagrams and layout representations, Interconnect modeling: resistance, capacitance, and delay considerations, Interconnect scaling, signal integrity, and crosstalk effects.

UNIT-IV POWER OPTIMIZATION AND SEQUENTIAL DESIGN

Power dissipation components in CMOS circuits: dynamic, static, and short-circuit power, Power estimation and reduction techniques, Design and analysis of CMOS latches and flip-flops, Timing parameters: setup time, hold time, clock skew, and static timing analysis.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V DATAPATH AND APPROXIMATE COMPUTING SUBSYSTEM

Design of arithmetic subsystems: adders and related datapath elements, Approximate computing concepts and design trade-offs, Error metrics and performance evaluation in approximate subsystems, Case studies on power-performance-accuracy optimization.

TEXT BOOKS:

1. 1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikoli??, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2016.
2. 2. Neil H.E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, 2015.
3. 3. S.M. Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 4th Edition, McGraw-Hill Education, 2019.

REFERENCE BOOKS:

1. 1. Kiat-Seng Yeo & Kaushik Roy, Low-Voltage, Low-Power VLSI Subsystems, McGraw-Hill Professional, 2004.
2. 2. Kaushik Roy & Sharat C. Prasad, Low-Power CMOS VLSI Circuit Design, John Wiley & Sons, 2000.
3. 3. Ajit Pal, Low-Power VLSI Circuits and Systems, Springer India, 2015.
4. 4. Ming-Bo Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective, CRC Press, 2012.

COURSE OUTCOMES:

1. 1. Introduce the fundamental design metrics-delay, power, and area-in Digital CMOS VLSI subsystem design.
2. 2. Develop the ability to estimate and optimize power consumption in CMOS logic circuits and interconnects.
3. 3. Analyze interconnect-aware design challenges and explore strategies for delay and energy optimization in subsystems
4. 4. Familiarize students with approximate computing concepts, datapath subsystem design, and associated error metrics.
5. 5. Explain the design principles, timing parameters, and trade-offs involved in sequential circuit elements such as latches and flip-flops.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(25D57204C) ALGORITHMS FOR VLSI DESIGN (PE-IV)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To impart knowledge about the computer arithmetic algorithms, including different techniques enabling enhanced throughput and low power.
2. To understand algorithms techniques to hardware implementation of various arithmetic operations.

UNIT-I NUMBERS AND ARITHMETIC

Review of Number Systems, Their Encoding, and Basic Arithmetic Operations. Class of Fixed-Radix Number Systems and Unconventional Fixed-Point Number Systems. Representing Signed Numbers, Negative-Radix Number Systems, Redundant Number Systems, and Residue Number Systems.

UNIT-II ALGORITHMS FOR FAST ADDITION

Basic Addition and Counting, Bit-Serial and Ripple-Carry Adders, Addition of a Constant (Counters), Manchester Carry Chains and Adders, Carry-Look-Ahead Adders, Carry Determination as Prefix Computation, and Alternative Parallel Prefix Networks. VLSI Implementation Aspects, Variations in Fast Adders, Simple Carry-Skip and Carry-Select Adders, Hybrid Adder Designs, and Optimizations in Fast Adders. Multi-Operand Addition, Wallace and Dadda Trees, Parallel Counters, Generalized Parallel Counters, and Adding Multiple Signed Numbers.

UNIT-III HIGH-SPEED MULTIPLICATION

Basic Multiplication Schemes, Shift/Add Multiplication Algorithms, Programmed Multiplication, and Basic Hardware Multipliers. Multiplication of Signed Numbers and Multiplication by Constants. Overview of Fast Multipliers, High-Radix Multipliers, Modified Booth???s Recoding, Tree and Array Multipliers, Variations in Multipliers, and VLSI Layout Considerations.

UNIT-IV FAST DIVISION AND DIVISION THROUGH MULTIPLICATION

Basic Division Schemes, Shift/Subtract Division Algorithms, Programmed Division, Restoring and Non-Restoring Hardware Dividers, and Signed Division. Division by Constants, Fast Divider Techniques, High-Radix Dividers, Variations in Dividers, Combined Multiply/Divide Units, Division by Convergence, and Hardware Implementation Approaches.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V REAL ARITHMETIC AND IMPLEMENTATION TOPICS

Representing Real Numbers, Floating-Point Arithmetic, ANSI/IEEE Floating-Point Standard, Exceptions and Features, Floating-Point Arithmetic Operations, and Rounding Schemes. Logarithmic Number Systems, Floating-Point Adders, Barrel-Shifter Design, Leading-Zeros/Ones Counting, Floating-Point Multipliers and Dividers. Arithmetic Errors and Error Control, Computing Algorithms, Exponentiation, Approximating Functions, Merged Arithmetic, Arithmetic by Table Lookup, Trade-offs in Cost, Speed, and Accuracy, High-Throughput Arithmetic, Low-Power Arithmetic, Fault-Tolerant Arithmetic, Emerging Trends, and Impact of Hardware Technology.

TEXT BOOKS:

1. Computer Arithmetic: Algorithms and Hardware Design by Parhami, B., Oxford University Press
2. Computer Arithmetic Algorithms by Koren, I., CRC Press

REFERENCE BOOKS:

1. Digital Arithmetic by Ercegovac, M. and Lang, T., Elsevier.
2. Verilog Digital Computer Design Algorithms into Hardware by Mark Gordon Arnold, Prentice Hall PTR. Zhang, L., and Joshi, R. V., Interconnect Analysis and Design for Advanced VLSI, Springer, 201

COURSE OUTCOMES:

1. Understand hardware implementation of various algorithms.
2. Learn to apply tradeoffs and multiple implementations and architectures.
3. Know the use cases of various algorithms and their considerations

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	2

(25D57204D) LOW POWER VLSI DESIGN (PE-IV)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. 2. To implement Low power design approaches for system level and circuit level measures.
3. 3. To design low power adders, multipliers and memories for efficient design of systems.

UNIT-I FUNDAMENTALS

Need for Low Power Circuit Design, Sources of Power Dissipation Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II LOW-POWER DESIGN APPROACHES

Low-Power Design through Voltage Scaling VTCMOS circuits, MTCMOS circuits, Architectural Level Approach Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III LOW-VOLTAGE LOW-POWER ADDERS

Introduction, Standard Adder Cells, CMOS Adders Architectures. Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques. Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles

UNIT-IV LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. 1. CMOS Digital Integrated Circuits Analysis and Design Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. 2. Low-Voltage, Low-Power VLSI Subsystems Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. 1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective Ming-BO Lin, CRC Press, 2011.
2. 2. Low Power CMOS Design Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. 3. Low Power CMOS VLSI Circuit Design Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

e-Resources and Digital Material:

COURSE OUTCOMES:

1. 1. Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect.
2. 2. Design Low power design approaches for system level and circuit level measures.
3. 3. Design and evaluate low power adders for efficient design of systems.
4. 4. Design and evaluate low power multipliers for efficient design of systems.
5. 5. Design and evaluate low power memories for efficient design of systems.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	2

(25D57204E) VLSI SIGNAL PROCESSING (PE-IV)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. To study the existing architectures suitable for VLSI
2. 2. To understand the concepts of folding and unfolding algorithms and applications
3. 3. To design new architectures suitable for VLSI.
4. 4. To implement fast convolution algorithms

UNIT-I INTRODUCTION TO DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT-II FOLDING AND UNFOLDING

Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT-III SYSTOLIC ARCHITECTURE DESIGN

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT-IV FAST CONVOLUTION

Introduction Cook - Toom Algorithm Winogard algorithm Iterated Convolution Cyclic Convolution Design of Fast Convolution algorithm by Inspection.

UNIT-V LOW POWER DESIGN

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipelines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. 1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998
2. 2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985

REFERENCE BOOKS:

1. 1. Jose E. France, Yannis Tsividis, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994
2. 2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

COURSE OUTCOMES:

1. 1. To study the existing architectures suitable for VLSI.
2. 2. To understand the concepts of folding and unfolding algorithms and applications.
3. 3. To design new architectures suitable for VLSI.
4. 4. To implement fast convolution algorithms.
5. 5. To apply low power approaches in the VLSI design for the signal processing.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(25D57205) CMOS MIXED SIGNAL IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To design and simulate op-amp for given specifications.
2. To design and simulate data converter for given specifications.
3. To design and simulate PLL and VCO for given specifications.
4. To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Cycle 1:

Fully compensated op-amp with resistor and miller compensation

High speed comparator design

Two stage cross coupled clamped comparator.

Strobed Flip-flop

Data converter

Cycle 2:

Switched capacitor circuits

Parasitic sensitive integrator

Parasitic insensitive integrator

Design of PLL

Design of VCO

Band gap reference circuit

Layouts of All the circuits Designed and Simulated

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Design and simulate op-amp for given specifications
2. Design and simulate data converter for given specifications
3. Design and simulate switched capacitor filters
4. Design and simulate PLL and VCO for given specifications
5. Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(25D57206) PHYSICAL DESIGN AUTOMATION LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To learn the implementation of different Physical Design Automation algorithms
2. To implement different graph algorithms
3. To implement different partitioning algorithms
4. To implement different floor planning algorithms
5. To implement different routing algorithms

Cycle 1:

Graph algorithms

Graph search algorithms

Depth first search

Breadth first search

Spanning tree algorithm

Kruskals algorithm

Shortest path algorithm

Dijkstra algorithm

Floyd- Warshall algorithm

Steiner tree algorithm

Computational geometry algorithm

Line sweep method

Extended line sweep method

Cycle 2:

Partitioning algorithms

Group migration algorithms

i. Kernighan Lin algorithm

Extensions of Kernighan-Lin algorithm

Fiduccias Mattheyses algorithm

Goldberg and Burstein algorithm

Simulated annealing and evolution algorithms

Simulated annealing algorithm

Simulated evolution algorithm

iii) Metric allocation method

Floor planning algorithms

Constraint based methods

Integer programming based methods

Rectangular dualization based methods

Hierarchical tree based methods

Simulated evolution algorithms

Time driven Floor planning algorithms

Routing algorithms

Two terminal algorithms

Maze routing algorithms

Lees algorithm

Soukups algorithm

Hadlock algorithm

Line-Probe algorithm

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Learn the implementation of different Physical Design Automation algorithms
2. Implement different graph algorithms
3. Implement different partitioning algorithms
4. Implement different floor planning algorithms
5. Implement different routing algorithms

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
2	0	0	2

(25D57207) QUANTUM TECHNOLOGIES AND APPLICATIONS

Course Category	**Mandatory Course (credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. Introduce fundamental quantum concepts like superposition and entanglement
2. 2. Understand theoretical structure of qubits and quantum information
3. 3. Explore conceptual challenges in building quantum computers.
4. 4. Explain principles of quantum communication and computing
5. 5. Examine real-world applications and the future of quantum technologies

UNIT-I INTRODUCTION TO QUANTUM THEORY AND TECHNOLOGIES

The transition from classical to quantum physics, Fundamental principles explained conceptually: Superposition, Entanglement, Uncertainty Principle, Wave-particle duality, Classical vs Quantum mechanics-theoretical comparison, Quantum states and measurement: nature of observation, Overview of quantum systems: electrons, photons, atoms, The concept of quantization: discrete energy levels, Why quantum? Strategic, scientific, and technological significance, A snapshot of quantum technologies: Computing, Communication, and Sensing, National and global quantum missions: India???s Quantum Mission, EU, USA, China.

UNIT-II THEORETICAL STRUCTURE OF QUANTUM INFORMATION SYSTEMS

What is a qubit? Conceptual understanding using spin and polarization, Comparison: classical bits vs quantum bits, Quantum systems: trapped ions, superconducting circuits, photons (non-engineering view),Quantum coherence and decoherence ??? intuitive explanation, Theoretical concepts: Hilbert spaces, quantum states, operators ??? only interpreted in abstract, The role of entanglement and non-locality in systems, Quantum information vs classical information: principles and differences, Philosophical implications: randomness, determinism, and observer role.

UNIT-III BUILDING A QUANTUM COMPUTER ??? THEORETICAL CHALLENGES AND REQUIREMENTS

is What a qubit? Conceptual understanding using spin and polarization, Comparison: classical bits vs quantum bits, Quantum systems: trapped ions, superconducting circuits, photons (non-engineering view),Quantum coherence and decoherence ??? intuitive explanation, Theoretical concepts: Hilbert spaces, quantum states, operators ??? only interpreted in abstract, The role of entanglement and non-locality in systems, Quantum information vs classical information: principles and differences, Philosophical implications: randomness, determinism, and observer role.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV QUANTUM COMMUNICATION AND COMPUTING-THEORETICAL PERSPECTIVE

Quantum vs Classical Information, Basics of Quantum Communication, Quantum Key Distribution (QKD),Role of Entanglement in Communication, the Idea of the Quantum Internet ??? Secure Global Networking, Introduction to Quantum Computing, Quantum Parallelism (Many States at Once),Classical vs Quantum Gates, Challenges: Decoherence and Error Correction, Real-World Importance and Future Potential.

UNIT-V APPLICATIONS, USE CASES AND THE QUANTUM FUTURE

Real-world application domains: Healthcare (drug discovery),Material science, Logistics and optimization, Quantum sensing and precision timing, Industrial case studies: IBM, Google, Microsoft, Quantum, Ethical, societal, and policy considerations, Challenges to adoption: cost, skills, standardization, Emerging careers in quantum: roles, skillsets, and preparation pathways, Educational and research landscape ??? India's opportunity in the global quantum race.

TEXT BOOKS:

1. 1. Michael A. Nielsen, Isaac L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 10th Anniversary Edition, 2010.
2. 2. Eleanor Rieffel and Wolfgang Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011.
3. 3. Chris Bernhardt, Quantum Computing for Everyone, MIT Press, 2019

REFERENCE BOOKS:

1. 1. David McMahon, Quantum Computing Explained, Wiley, 2008
2. 2. Phillip Kaye, Raymond Laflamme, Michele Mosca, An Introduction to Quantum Computing, Oxford University Press, 2007.
3. 3. Scott Aaronson, Quantum Computing Since Democritus, Cambridge University Press, 2013
4. 4. Alastair I.M. Rae, Quantum Physics: A Beginner's Guide, Oneworld Publications, Revised Edition, 2005
5. 5. Eleanor G. Rieffel, Wolfgang H. Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011
6. 6. Leonard Susskind, Art Friedman, Quantum Mechanics: The Theoretical Minimum, Basic Books, 2014
7. 7. Bruce Rosenblum, Fred Kuttner, Quantum Enigma: Physics Encounters Consciousness, Oxford University Press, 2nd Edition, 2011

COURSE OUTCOMES:

1. .Explain core quantum principles in a non-mathematical manner.
2. Compare classical and quantum information systems
3. Identify theoretical issues in building quantum computers

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

---

4. Discuss quantum communication and computing concepts
5. .Recognize applications, industry trends, and career paths in quantum technology

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem. L T P C

(25D57208) COMPREHENSIVE VIVA VOCE

Course Category	
Course Enrichment Relevance	

COURSE OBJECTIVES:

Real-world application domains: Healthcare (drug discovery),Material science, Logistics and optimization, Quantum sensing and precision timing, Industrial case studies: IBM, Google, Microsoft, Quantum, Ethical, societal, and policy considerations, Challenges to adoption: cost, skills, standardization, Emerging careers in quantum: roles, skillsets, and preparation pathways, Educational and research landscape ??? India’s opportunity in the global quantum race.

COURSE OUTCOMES:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209A) ENTREPRENEURSHIP ESSENTIALS (AC-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

UNIT-I FOUNDATIONS OF ENTREPRENEURSHIP

Introduction to Entrepreneurship, Case Studies: Dhirubhai Ambani & Sofia, Myths and Realities about Entrepreneurship, Entrepreneurial Qualities and Mindset, Mission and Vision Development, Why Start-ups Fail? ??? Common Pitfalls and Lessons Learned

UNIT-II BUSINESS MODELS AND STRATEGIC PLANNING

Value Proposition and Opportunity Identification, Business Model Canvas and Business Model Generation, Competitive Advantage and Lean Start-up Methodology, Team Formation and Early Recruitment, Legal Forms of Business and Organizational Structure.

UNIT-III MARKETING, FINANCE, AND BUSINESS PLANNING

Marketing Management Principles for Start-ups, Market Research: Methods, Data Analysis, and Case Studies, Financial Statements: P&L, Balance Sheet, and Cash Flow, Cost-Volume-Profit Analysis and Break-even Analysis, Capital Budgeting and Financial Decision Making, Business Plan Preparation and Pitching Techniques

UNIT-IV INNOVATION, FUNDING, AND LEGAL FRAMEWORK

Innovation Strategies: Design Thinking, TRIZ, Open Innovation, Government Incentives and Support Systems for Entrepreneurs, Incubation and Acceleration Programs, Funding Sources: Bootstrapping, Crowdfunding, Angel Investors, Venture Capital, Debt Financing, Due Diligence and Project Cost Management, Legal Aspects: IPR, GST, and Labor Laws

UNIT-V GROWTH, HUMAN RESOURCE, AND RISK MANAGEMENT

Growth Hacking and Business Scaling Strategies, Human Resource Management in Start-ups, Negotiation Skills and Leadership Development, Pivoting Strategies and Entrepreneurial Case Studies, Risk Assessment and Strategic Management for Start-ups, Success and Failure Factors in Entrepreneurial Ventures

TEXT BOOKS:

1. Effective Entrepreneurial Management: Strategy, Planning, Risk Management, and Organization - Robert D. Hisrich ??? Veland Ramadani, Springer (2017)

2. Entrepreneurship- Theory, Process Practice ???by Kuratko &Hodgetts, Thompson South-Western Publication
3. Entrepreneurship ???by Robert D. Hisrich (Edition-9)

COURSE OUTCOMES:

1. Explain the stages in the entrepreneurial venture life-cycle and the critical decisions involved in each stage.
2. Identify, evaluate, and select potential business opportunities using structured entrepreneurial frameworks.
3. Demonstrate the ability to prepare basic financial statements, project reports, and feasibility analyses for start-up ventures
4. Apply management principles ??? marketing, HR, and strategic planning ??? in designing and managing small or emerging enterprises.
5. Analyze funding options, risk factors, and legal aspects to support sustainable and ethical entrepreneurial ventures

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209B) PEDAGOGY STUDIES (AC-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. 1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. 2. Identify critical evidence gaps to guide the development.

UNIT-I INTRODUCTION AND METHODOLOGY

Aims and Rationale, Policy Background, Conceptual Framework and Terminology, Theories of Learning, Curriculum, Teacher Education, Conceptual Framework, Research Questions, Overview of Methodology, and Searching.

UNIT-II THEMATIC OVERVIEW

Pedagogical Practices being used by teachers in formal and informal classrooms in developing countries, Curriculum, and Teacher Education.

UNIT-III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES, METHODOLOGY FOR THE IN DEPTH STAGE

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the echo curriculum and guidance materials best support effective pedagogy. Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers??? attitudes and beliefs and Pedagogic strategies.

UNIT-IV PROFESSIONAL DEVELOPMENT

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V RESEARCH GAPS AND FUTURE DIRECTIONS

Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

TEXT BOOKS:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

---

1. 1. AckersJ, HardmanF(2001)Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. 2. AgrawalM(2004)Curricular reform in schools: The importance of evaluation, Journal of 3. Curriculum Studies, 36 (3): 361-379.
3. 4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. 5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count International Journal Educational Development, 33 (3): 272282.
5. 6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell. Chavan M (2003) Read India: A mass scale, rapid, learning to read campaign. 7. www.pratham.org/images/resource%20working%20paper%202.pdf.

REFERENCE BOOKS:

e-Resources and Digital Material:

COURSE OUTCOMES:

1. 1. Understand and explain the foundational aspects of education including aims, rationale, policy background, theories of learning, curriculum design, and teacher education methodologies.
2. 2. Identify and analyze various pedagogical practices adopted in formal and informal classroom settings in developing countries, and evaluate their implications for curriculum and teacher education.
3. 3. Evaluate evidence-based research on the effectiveness of pedagogical practices and examine how teacher education, curriculum, and professional materials can support effective pedagogy through a strong theoretical and methodological framework.
4. 4. Assess and apply principles of professional development, focusing on classroom alignment, peer and community support, and overcoming barriers such as limited resources and large class sizes.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209C) YOGA FOR STRESS MANAGEMENT (AC-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

UNIT-I DEFINITIONS OF EIGHT PARTS OF YOGA (ASHTANGA)

Definitions and explanation of the eight parts of Yog (Ashtanga): Yama, Niyama, Asana, Pranayama, Pratyahara, Dharana, Dhyana, and Samadhi. Understanding the holistic approach of Ashtanga Yog in managing stress and achieving mental balance.??

UNIT-II YAM AND NIYAM

Detailed study of Yam and Niyam ??? their meaning, importance, and practical application in daily life. Understanding how ethical and personal disciplines help in stress reduction and personality development.??

UNIT-III DO???S AND DON???TS IN LIFE

i) Yam (Do???s): Ahimsa, Satya, Astheya, Brahmacharya, and Aparigraha. ii) Niyam (Don???ts): Shaucha, Santosha, Tapa, Swadhyaya, and Ishwar Pranidhana. Emphasis on self-discipline, moral conduct, and positive thinking as tools for peaceful living and stress control.

UNIT-IV ASAN AND PRANAYAM

Introduction to Asanas (Postures) and Pranayam (Breathing Techniques). Importance of physical postures and controlled breathing in maintaining physical fitness, mental calmness, and emotional stability.

UNIT-V VARIOUS YOGA POSES AND THEIR BENEFITS FOR MIND & BODY

i) Study of various Yog poses and their specific benefits for the mind and body. ii) Regularization of breathing techniques and their physiological and psychological effects. Types of Pranayam: Anulom Vilom, Bhastrika, Kapalbhati, Bhramari, and others.

TEXT BOOKS:

1. Yogic Asanas for Group Training-Part-I: Janardan Swami Yoga bhyasiMandal, Nagpur
2. Rajayogaor conquering the Internal Nature by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

REFERENCE BOOKS:

e-Resources and Digital Material:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
2	0	0	0

(25D57209D) CONSTITUTION OF INDIA (AC-II)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To help students understand the basic features, principles, and structure of the Indian Constitution.
2. To familiarize students with the fundamental rights, duties, and directive principles that form the foundation of Indian democracy
3. To understand the roles and responsibilities of the Union and State governments, and the functioning of the judiciary
4. To develop awareness of the constitutional provisions related to governance, policy-making, and administration
5. To inspire students to be responsible citizens by understanding their constitutional rights and duties

UNIT-I INTRODUCTION TO THE CONSTITUTION OF INDIA

Historical Background-Making of the Constitution-Preamble to the Constitution-Salient Features of the Constitution-The Union and Its Territory-Citizenship ??? Fundamental Rights and Fundamental Duties ??? Directive Principles of State Policy.

UNIT-II UNION GOVERNMENT AND ITS ADMINISTRATION STRUCTURE OF THE INDIAN UNION –

Structure of the Indian Union – Powers and Functions of the President, Vice President, Prime Minister, Council of Ministers, and Parliament – Cabinet Committees – Role and Responsibilities of the Prime Minister’s Office – Lok Sabha and Rajya Sabha: Composition, Powers, and Functions.

UNIT-III STATE GOVERNMENT AND ITS ADMINISTRATION GOVERNOR ???

Governor ??? Chief Minister ??? Council of Ministers ??? State Legislature ??? High Courts and Subordinate Courts ??? Special Status of Jammu & Kashmir and other States ??? Centre-State Relations ??? Administration of Union Territories.

UNIT-IV LOCAL GOVERNANCE AND CONSTITUTIONAL BODIES

Panchayati Raj Institutions: 73rd and 74th Constitutional Amendments – Urban and Rural Local Bodies – Election Commission – Union and State Public Service Commissions – Finance Commission – Comptroller and Auditor General of India – Attorney General and Advocate General.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V CONSTITUTIONAL AMENDMENTS AND EMERGENCY PROVISIONS

Amendment Procedure ??? Major Amendments and Their Significance ??? Emergency Provisions: National, State, and Financial Emergencies ??? Judicial Review and Independence of Judiciary ??? Right to Information Act ??? Role of the Constitution in Nation Building and Citizen Empowerment.

TEXT BOOKS:

1. Dr. J. N. Pandey, The Constitutional Law of India, Central Law Agency, 2022.
2. D.D. Basu, Introduction to the Constitution of India, LexisNexis, 25th Edition, 2021.
3. M. Laxmikanth, Indian Polity, McGraw Hill Education, 7th Edition, 2023.
4. Granville Austin, The Indian Constitution: Cornerstone of a Nation, Oxford University Press, 2014.
5. Subhash Kashyap, Our Constitution: An Introduction to India???s Constitution and Constitutional Law, National Book Trust, India, 2018.

REFERENCE BOOKS:

COURSE OUTCOMES:

1. Understand the key elements, philosophy, and evolution of the Indian Constitution.
2. Describe the structure and functioning of the Union, State, and Local Governments.
3. Analyze the importance of Fundamental Rights, Duties, and Directive Principles in ensuring social justice
4. Recognize the role of various constitutional bodies and their impact on governance
5. Develop a sense of civic responsibility, constitutional awareness, and commitment to national integrity and harmony.

SANTHIRAM ENGINEERING COLLEGE, NANDYAL
(AUTONOMOUS)

VISION

- To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

MISSION

M1: To provide Advanced Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization by arising a self-sustained University.

M2: To establish postgraduate programs in the current and Advanced Technologies.

M3: To establish an R&D Consultancy through developing Industry Institute Interaction, building up exceptional infrastructure.

M4: To propel every individual, realize and act for the technical development of the society

MOTTO

- Education for Peace and Progress

+91 9866308475

www.srecnandyal.edu.in

NH-40, NANDYAL-518501,
NANDYAL(Dist), A.P