SANTHIRAM ENGINEERING COLLEGE
(AUTONOMOUS)

Approved by A.I.C.T.E., New Delhi, Permanently Affiliated to JNT University, Ananthapuramu;
Accredited by NAAC with Grade-A, Accredited by NBA (ECE & CSE);
An ISO 9001:2015 Certified Institution, 2(f) & 12(B) recognition by UGC Act, 1956
NH-40, Nandyal-518501, Nandyal (Dist), A.P.

learn-Grow-Empower

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.TECH (ECE-VLSI SD)

REGULAR TWO YEAR PG DEGREE COURSE

(Applicable for the Admitted Batch 2025-26)

REGULATIONS: R-25

SANTHIRAM ENGINEERING COLLEGE : NANDYAL

ACADEMIC RULES & REGULATIONS

(Effective for the students admitted into I year from the Academic Year 2025-2026)

Santhiram Engineering College, Nandyal (SREC) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M. Tech) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Santhiram Engineering College, Nandyal (SREC) shall confer M. Tech degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. Award of the M. Tech Degree

A student will be declared eligible for the award of the M. Tech degree if he/she fulfils the following:

1.1 Pursues a course of study for not less than two academic years and not more than four academic years.

1.2 Registers for 75 credits and secures all 75 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M. Tech course and their admission stands cancelled.

3. Programme of Study:

The following M. Tech Specializations are offered at present in different branches of Engineering and Technology in non-autonomous affiliated colleges:

S.No.	Discipline	Name of the Specialization	Code
01	Electronics and Communication Engineering	Embedded Systems	55
		VLSI System Design	57
02	Computer Science and Engineering	Computer Science & Engineering	58
		CSE (Artificial Intelligence & Machine Learning)	13

4. Eligibility for Admissions:

4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.

4.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M. Tech programmes an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. Programme related terms:

5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for students to select from the prescribed courses.

6. Programme Pattern:

6.1 Total duration of the of M. Tech programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M. Tech degree programme are broadly classified as follows:

S. No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/department/ branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Mandatory Course	Quantum Technology and Application	To understand importance of latest technologies, research and process of creation of patents through research
		Research methodology & IPR	
4.		Skill Enhancement courses (SE)	Interdisciplinary / job-oriented/domain courses which are relevant to the industry
		Comprehensive Viva	To test the overall domain knowledge
		Short Term Industry Internship	To provide real time exposure
		Dissertation	To provide application of domain knowledge to solve real problems
5.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners.

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

7.1 A student shall be eligible to appear for the external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction period. The other 10 marks is awarded for continuous assessment in the form of assignments, quizzes, open book examination, presentation, etc. First mid examination shall be conducted for I & II units of the syllabus and second mid

examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) and each question carries 10 marks. Final Internal marks for a total of 40 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.
ii. All the questions have to be answered compulsorily.
iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.

The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15.

8.5 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re- examination shall be conducted for failed candidates for 40 marks for every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.7 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.8 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the Institution norms and shall be produced to the Committees of the University as and when the same are asked for.

9. Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the Institution shall allow up to a maximum of 40% of the Professional and Open Electives in a semester through SWAYAM/SWAYAM Plus.

9.1 The Institution shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 Students may register for an 8-week (2 credits) or 12-week (3 credits) SWAYAM / SWAYAM plus course with the approval of the Head of the Department (HoD).

9.7 Examination fees, if applicable, shall be borne by the student. Pass marks and grading will be as per the Institution academic regulations.

9.8 A student must get minimum 40% marks for assignments and quizzes on the SWAYAM/ SWAYAM plus platform to be eligible for the end-semester examination. The students who are unable to get minimum internal marks in SWAYAM/ SWAYAM plus platform, they have to re-register for the course in subsequent semester through SWAYAM/ SWAYAM plus platform.

9.9 The end-semester exam may be conducted by the National Testing Agency (NTA), the National Programme on Technology Enhanced Learning (NPTEL) or the Institution during the regular end-term exams. Evaluation shall comprise 60% weightage for the end-semester examination and 40% for assignments and quizzes conducted by the SWAYAM/ SWAYAM plus course coordinator. The student has to get 50% marks for internal and external with minimum of 40% marks in the external examination to declare them as pass.

9.10 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester. However, the credits will be transferred to the students who got minimum 50% marks with 40% marks in the external examination

9.11 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.12 The Institution shall ensure no overlap of SWAYAM MOOC exams with that of the Institution examination schedule. In case of delay in SWAYAM results, the Institution will re-issue the marks sheet for such students.

9.13 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the minimum 50% of marks and grades.

9.14 The respective Departments shall submit the following to the examination section of the Institution:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.15 The Institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only

after seeking approval of the Institution/University at least three months prior to the commencement of the semester.

10. Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For each theory subject, the candidate has to pay the requisite fee along with the requisition through concerned Head of the department.

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Progress of the project work is monitored through three reviews:

- Project review – I at the beginning of the III semester for zero marks
- Project review – II at the end of the third semester for 100 marks
- Project review – III before submission of the thesis i.e., end of the IV semesters for 100 marks

External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M. Tech programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.3 Project work shall be carried out under the supervision of teacher in the parent department concerned.

11.4 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases, one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/

external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry‟s or R&D laboratory‟s own interests. A certificate from the external supervisor is to be included in the dissertation.

11.5 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.6 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.7 After registration, a candidate must present in Project Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.8 The Project Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.9 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - II. Only after successful completion of Project Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Review - II shall reappear after three months.

11.10 The Project Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Review - III. If student fails to obtain the required minimum marks, he/she has to reappear for Project Review - III after a month.

11.11 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.12 After approval from the PRC, the student is permitted to submit a report. The dissertation report will be accepted only when the plagiarism is within 30% checked through Turnitin software (repository mode). The plagiarism report shall be submitted along with the dissertation report.

11.13 Research paper related to the Project Work shall be published in an SCI/ESCI/Scopus/UGC Care listed journal, or in conference proceedings with ISBN number organized by professional societies such as IEEE, IEI, etc.

11.14 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.15 The dissertation shall be adjudicated by an external examiner selected by the Institution. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each student. However, the dissertation will be adjudicated by one examiner nominated by the Head of the Institution.

11.16 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after the approval from the Institution.

11.17 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.18 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

11.19 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12. Industry Internships:

Industry internship either onsite or virtual with a minimum of 06-08 weeks" duration, done at the end of 1st year second semester. It shall be completed in collaboration with local industries, Govt. Organizations, construction agencies, Power projects, software MNCs or any industries in the areas of concerned specialization of the PG program. The student shall register for the internship as per course structure after commencement of academic year.

Evaluation of the summer internships shall be through the departmental committee. A student will be required to submit a summer internship report to the concerned department and appear for an oral presentation before the departmental committee comprising of Head of the Department, Mentor/Supervisor of the internship and a senior faculty member of the department. A certificate of successful completion from industry shall be included in the report. Internship will be evaluated for 100 marks with 50 marks for the report evaluated by the mentor and 50 marks for oral presentation. A student should secure minimum 50% of marks for successful completion. In case, if a student fails, he/she shall reappear as and when semester supplementary examinations are conducted by the Institution.

13. Comprehensive Viva

A Comprehensive Viva shall be conducted after the II Semester examinations for 100 marks by a committee consisting of the Head of the Department, one senior faculty member of the same specialization, and an external subject expert appointed by the Head of the Institution. The student must secure a minimum of 50% marks to be declared as passed

14. Credits for Co-curricular Activities

The college shall be introducing Co-Curricular activities in IV semester with One credit. The student must be participating in Co-Curricular / extra-curricular activities such as publishing a paper or participating in a National / International workshops / symposium / seminar / training organized by any private institution / Govt. organization / Training centers in virtual/offline mode. The student has to participate in Co-Curricular activities during their program duration and submit the certificate at the end of the IV semester. If he/she fails to submit will not be eligible for the award of degree. In such cases, the student shall repeat and submit the Co-Curricular activity.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	**Maximum Credits / Activity**
Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student)	0.5
Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student)	1
Academic Award/Research Award from State Level/National Agencies	0.5
Academic Award/Research Award from International Agencies	1
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	0.5
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	1

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit. A minimum participation of five days is required to earn the necessary credits. Alternatively, the student may attend five different one day programs to meet this requirement.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

15. Grading:

As a measure of the student‟s performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

i) A student obtaining Grade „F‟ or Grade „Ab‟ in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.

ii) For noncredit audit courses, “Satisfactory” or “Unsatisfactory” shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i) / \Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i) / \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

16. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	CGPA to be secured
First Class with Distinction	≥7.5%
First Class	< 7,5≥ 6.5
Pass Class	< 6.5

17. Exit Policy:

The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

18. Withholding of Results:

If the candidate has any case of in-discipline pending against him/her, the result of the candidate shall be withheld, and he/she will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

19. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been

detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

20. General:

20.1 The academic regulations should be read as a whole for purpose of any interpretation.

20.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

20.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.

20.4 Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

20.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

20.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

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RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and handed over to the examination of the autonomous college.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all examinations, if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty inor outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations / Assistant Controller of Examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ Controller of Examinations / Assistant Controller of Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
3. A show cause notice shall be issued to the college.
4. Impose a suitable fine on the college.
5. Shifting the examination centre from the college to another college for a specific period of not less than one year.

Note:-

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil allthe norms required for the award of Degree.

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SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
I-Semester Course Structure

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem. - Course Structure

S.No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				Lecture	Tutorial	Practical	Credits	Internal	External	Total
1	25D57101	PC	CMOS ANALOG IC DESIGN	3	0	0	3	40	60	100
2	25D57102	MC(C)	CMOS DIGITAL IC DESIGN	3	0	0	3	40	60	100
3	25D57103A	PE	CAD FOR VLSI (PE-I)	3	0	0	3	40	60	100
4	25D57103B	PE	MICROCHIP FABRICATION TECHNIQUES (PE-I)	3	0	0	3	40	60	100
5	25D57103C	PE	SCRIPTING LANGUAGES FOR VLSI (PE-I)	3	0	0	3	40	60	100
6	25D57103D	PE	NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)	2	0	0	3	40	60	100
7	25D57103E	PE	MEMS AND NEMS (PE-I)	3	0	0	3	40	60	100
8	25D57104A	PE	ASIC DESIGN (PE-II)	3	0	0	3	40	60	100
9	25D57104B	PE	FPGA ARCHITECTURES AND APPLICATIONS (PE-II)	3	0	0	3	40	60	100
10	25D57104C	PE	DEEP LEARNING FOR VLSI (PE-II)	3	0	0	3	40	60	100
11	25D57104D	PE	DEVICE MODELLING (PE-II)	3	0	0	3	40	60	100
12	25D57104E	PE	MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)	3	0	0	3	40	60	100
13	25D57105	PC	CMOS ANALOG IC DESIGN LAB	0	0	4	2	40	60	100
14	25D57106	PC	CMOS DIGITAL IC DESIGN LAB	0	0	4	2	40	60	100
15	25D57107	MC(C)	RESEARCH METHODOLOGY AND IPR	2	0	0	2	40	60	100
16	25D57108	SC	RTL SYNTHESIS, SIMULATION AND VERIFICATION	0	1	2	2	40	60	100
17	25D57109A	MC(NC)	ENGLISH FOR RESEARCH PAPER WRITING (AC-I)	2	0	0	0	40	0	40
18	25D57109B	MC(NC)	VALUE EDUCATION (AC-I)	2	0	0	0	40	0	40
19	25D57109C	MC(NC)	DISASTER MANAGEMENT (AC-I)	2	0	0	0	40	0	40
20	25D57109D	MC(NC)	ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)	2	0	0	0	40	0	40

R-2025

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech
I -Semester Syllabus

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57101) CMOS ANALOG IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

UNIT-I MOS DEVICES AND MODELING

The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling -Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II ANALOG CMOS SUB-CIRCUITS

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage Band gap Reference.

UNIT-III CMOS AMPLIFIERS

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

UNIT-IV CMOS OPERATIONAL AMPLIFIERS

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT-V COMPARATORS

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce.

3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

COURSE OUTCOMES:

1. Understand significance of different biasing styles and apply them for designing analog ICs.
2. Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
3. Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57102) CMOS DIGITAL IC DESIGN

Course Category	**Mandatory Course (credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

UNIT-I MOS DESIGN PSEUDO NMOS LOGIC

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III SEQUENTIAL MOS LOGIC CIRCUITS

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.

COURSE OUTCOMES:

1. Design CMOS inverters with specified noise margins and propagation
2. Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
3. Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
4. Design basic combinational and sequential elements using NMOS and CMOS design strategies.
5. Analyze the dynamic performance of CMOS circuits

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103A) CAD FOR VLSI (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I INTRODUCTION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II PARTITIONING

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing

UNIT-III FLOOR PLANNING

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV PLACEMENT AND ROUTING & GLOBAL ROUTING AND DETAILED ROUTING

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms. Global Routing–Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing–Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing–Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

COURSE OUTCOMES:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement
3. Optimize the implemented design for area, timing and power by applying suitable constraints.
4. Practice the application of fundamentals of VLSI technologies
5. Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103B) MICROCHIP FABRICATION TECHNIQUES (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. Comprehend impact of semiconductor industry on the design of development of integrated circuits.
2. Acquaint with clean room technology
3. Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
4. Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
5. Understand packaging principles

UNIT-I INTRODUCTION TO PROCESSING

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction

UNIT-II PHOTOLITHOGRAPHY

Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT-III DIFFUSION & ION IMPLANTATION

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT-IV FILM DEPOSITIONS AND GROWTH

Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT-V YIELD

Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors. Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

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1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

COURSE OUTCOMES:

1. Understand various stages of fabrication
2. Understand various packaging techniques and Design rules
3. Understand the aspects of diffusion, ion implantation techniques.
4. Classify various thin films and its characteristics.
5. Specify NMOS and CMOS design rules corresponding to package operations.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103C) SCRIPTING LANGUAGES FOR VLSI (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To learn the fundamental syntax, control structures, file I/O, and data processing capabilities of PERL, TCL, and Python.
2. To apply Regular Expressions: Implement regular expressions in scripts to effectively parse and extract specific data from complex EDA tool reports and log files.
3. To automate EDA Tool Flow: Write scripts to control and automate EDA tools, managing workflows for simulation, synthesis, and other design-cycle tasks.
4. To develop VLSI Task Automation: Create efficient automation scripts to handle common VLSI design tasks, such as managing design files, generating reports, and checking for errors.
5. To select Appropriate Tools: Evaluate the requirements of a specific automation task and select the most appropriate scripting language (PERL, TCL, or Python) for the use case.

UNIT-I INTRODUCTION TO SCRIPTING LANGUAGES IN EDA

Introduction to scripting and automation, Scripting vs compiled languages, Using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops – overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

UNIT-II PERL SCRIPTING

Scalar data, Arrays and list data, Hashes, Input and output, Control structures, Regular expressions, Pattern matching with regex, Substitution and translation, Using files and file handles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

UNIT-III TCL SCRIPTING

Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV PYTHON FOR DESIGN AUTOMATION AND DATA PROCESSING

Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, Using os, sys, and subprocess modules, Writing utility scripts for automation

UNIT-V ADVANCED INTEGRATION AND COMPARISON

Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, Best practices for automation and maintainability, Calling external commands and shell integration in all three languages, Script interoperability using intermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks

REFERENCE BOOKS:

1. Robbins, Arnold. Scripting the UNIX System: Using Bash, Perl, and More. Addison-Wesley, 2003. g
2. Ousterhout, John K. Tcl and the Tk Toolkit. 2nd ed., Addison-Wesley Professional, 2009. 3. Python Software Foundation. Python Language Reference Manual. https://docs.python.or

COURSE OUTCOMES:

1. Describe the role of scripting languages in EDA workflows and differentiate between scripting and compiled languages.
2. Write PERL scripts to perform text parsing, data extraction, and report generation.
3. Develop TCL scripts to automate tool commands and control design processes in EDA tools.
4. Construct Python scripts for file handling, data processing, and automation of design-related tasks..
5. Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	3

(25D57103D) NANO-MATERIALS AND NANOTECHNOLOGY (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the basic idea behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and technologies for future applications.
3. To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT-I INTRODUCTION OF NANO MATERIALS AND NANOTECHNOLOGIES

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT-II FUNDAMENTALS OF NANOMATERIALS

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT-III MICRO-AND NANOLITHOGRAPHY TECHNIQUES

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT-IV INTRODUCTION & SYNTHESIS OF CNTS-ARC-DISCHARGE

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V FERROELECTRIC MATERIALS

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application

TEXT BOOKS:

1. Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2ndedition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGrawHill Education 2012.

REFERENCE BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI

COURSE OUTCOMES:

1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To Understand the advantages and Challenges of MEMS
4. To analyze the synthesis of CNTs with applications.
5. To acquire knowledge on the operation and characterization to achieve precisely designed systems

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57103E) MEMS AND NEMS (PE-I)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To introduce Nano-and Microsystems
2. To understand the modeling of micro and nano scale electromechanical systems

UNIT-I INTRODUCTION TO MEMS AND NEMS

MEMS and NEMS definitions, Taxonomy of Nano-and Microsystems-Synthesis and Design. Classification and considerations, Biomimetics, Biological analogies, and design–Biomimetics Fundamentals, Biomimetics for NEMS and MEMS,Nano-ICs and Nano computer architectures

UNIT-II MODELING OF MICRO AND NANO SCALE ELECTROMECHANICAL SYSTEMS

Introduction to modelling, analysis and simulation, basic electro-magnetic with application to MEMS and NEMS, modeling developments of micro-and nano actuators using electromagnetic-Lumped-parameter mathematical models of MEMS, energy conversion in NEMS and MEMS

UNIT-III MEMS FABRICATION TECHNOLOGIES

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation.Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching.

UNIT-IV MICROMACHINING

Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT-V NANOSYSTEMS AND QUANTUM MECHANICS

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TEXT BOOKS:

1. Sergey Edward Lyshevski, Lyshevski Edward Lyshevski, Nano-Electro Mechanical and Micro-Electro Mechanical Systems, Fundamental of Nano-and Micro-Engineering 2005, 2nd Ed., CRC Press.

2. A. S. Edelstein and Cammarata, Nanomaterials: Synthesis, Properties and Applications, 2002, Institute of Physics, Bristol, Philadelphia

REFERENCE BOOKS:

1. Kalantar-ZadehK, Nanotechnology Enabled Sensors, 2008, Springer.
2. Serge Luryi, Jimmy Xu, Alex Zaslavsky, Future trends in MicroElectronics,2007, John Wiley & Sons, Inc. Hoboken, New Jersey

e-Resources and Digital Material:

1. https://onlinecourses.nptel.ac.in/noc22_ee36/preview

COURSE OUTCOMES:

1. Acquire the knowledge of Nano- and Microsystems.
2. Identify the methods of modeling of micro and nano scale electromechanical
3. Ability to design the micro devices, micro systems using the MEMS fabrication process.
4. Gain a knowledge of basic approaches for micromachining
5. Develop experience on micro/nano systems for photonics.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104A) ASIC DESIGN (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand different types of ASICs and their libraries.
2. To understand about programmable ASICs, I/O modules and their interconnects.
3. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT-I INTRODUCTION TO ASICS

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT-II PROGRAMMABLE ASICS AND PROGRAMMABLE ASIC LOGIC CELLS

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT-IV LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT-V SIMULATION, TEST AND ASIC CONSTRUCTION

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

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TEXT BOOKS:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

REFERENCE BOOKS:

1. Himanshu Bhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001

COURSE OUTCOMES:

1. Understand different types of ASICs and their libraries.
2. Understand about programmable ASICs, I/O modules and their interconnects.
3. Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.
4. Understand the various Low Level Design Entry and Logic Synthesis
5. Analyze and Simulate the various Tests and ASIC Construction.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104B) FPGA ARCHITECTURES AND APPLICATIONS (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To acquire knowledge about various architectures and device technologies of PLD‟s
2. To comprehend FPGA Architectures
3. To analyze System level Design and their application for Combinational and Sequential Circuits
4. To familiarize with Anti-Fuse Programmed FPGAs
5. To apply knowledge of this subject for various design applications
6. To familiarize with SRAM FPGAs

UNIT-I INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III SRAM PROGRAMMABLE FPGA

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures

UNIT-IV ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT-V DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition

2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning

REFERENCE BOOKS:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

e-Resources and Digital Material:

1. http://www.digimat.in/nptel/courses/video/117108040/L01.html
2. https://www.youtube.com/watch?v=gCAYY0fHPq4

COURSE OUTCOMES:

1. Acquire knowledge about various architectures and device technologies of PLD‟s
2. Comprehend FPGA Architectures
3. Analyze System level Design and their applications for various architectures.
4. Familiarize with Anti-Fuse Programmed FPGAs
5. Apply knowledge of this subject for various design applications.
6. Familiarize with SRAM FPGAs

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1				2	2	2
CO2	3	3	2	1	2		2	2	2
CO3	3	2	2	1	3		2	2	2
CO4	3	2	2	1	2		2	2	2
CO5	3	3	3	2	3		2	2	2
CO6	3	2	2	1	2		2	2	2

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104C) DEEP LEARNING FOR VLSI (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To impart knowledge about the Artificial Neural networks and deep learning.
2. To introduce the fundamental concepts relevant to ANN architectures and deep learning algorithms.
3. To understand the applications and use cases of Deep Learning architectures for VLSI circuits and design automation.

UNIT-I INTRODUCTION TO DEEP LEARNING

History and evolution of Deep Learning; Fundamentals of Deep Learning; Training Deep Architectures; Intermediate Representations–Sharing Features and Abstractions across Tasks; Sigmoid Neurons; Gradient Descent; Feedforward Neural Networks; Dropout; Backpropagation – concepts and implementation.

UNIT-II DEEP LEARNING WITH TENSORFLOW

Introduction to Deep Learning and TensorFlow; How Deep Learning Works; Principal Component Analysis (PCA) and its Interpretations; Singular Value Decomposition (SVD); Greedy Layer-wise Pre-training; Improved Activation Functions; Weight Initialization Methods; Batch Normalization; Implementing Basic Deep Learning Models using TensorFlow.

UNIT-III DEEP LEARNING ALGORITHMS AND OPTIMIZATION

Gradient Descent and Backpropagation Techniques; Improving Deep Networks; Multi-Layer Neural Networks; The Challenge of Training Deep Neural Networks; Deep Generative Architectures; Mini-batches and Optimization Techniques; Handling Unstable Gradients; Regularization and Avoiding Over-fitting; Applying Deep Network Theory to Code Implementations.

UNIT-IV ADVANCED DEEP ARCHITECTURES

Introduction to Convolutional Neural Networks (CNNs) for Visual Recognition; Recurrent Neural Networks (RNNs); RNNs in Practice; Long Short-Term Memory (LSTM) and Gated Recurrent Unit (GRU) Architectures; LSTMs and GRUs in Practice; Reinforcement Learning; Importance of Unsupervised Learning; Training Auto encoders.

UNIT-V APPLICATIONS OF DEEP LEARNING IN VLSI

Deep Learning Applications in VLSI Design and Automation – Chip Design, Test Generation, Chip Testing, Diagnosis and Debug, and Characterization; AI-driven Design Flow Automation; Performance Prediction and Optimization in VLSI Circuits using Deep Neural Models.

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TEXT BOOKS:

1. Deep Learning: Methods and Applications by Li Deng and Dong Yu, now publisher.
2. Neural Networks and Deep Learning by Michael Nielsen, Determination Press.

REFERENCE BOOKS:

1. Hands-On Learning with Scikit-Learn and Tensorflow by Aurelien Geron, Oreilly.
2. Pattern Recognition and Machine Learning by Christopher Bishop, Springer-Verlag Berlin, Heidelberg.
3. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press.

COURSE OUTCOMES:

1. To Describe the key components of AI field and its relation and role in computer science.
2. To Build custom architectures from scratch
3. To be able to apply appropriate architectures for solving, modeling, optimizing and automizing VLSI related options.
4. To acquire the knowledge and experience of task level Communication in any Embedded System.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(25D57104D) DEVICE MODELLING (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the physics of 2-terminal MOS operation and its characteristics
2. To understand the physics of 4-terminal MOSFET operation and its characteristics.
3. To analyze the SOI MOSFET electrical characteristics.

UNIT-I 2-TERMINAL MOS DEVICE

Threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT-II C-V CHARACTERISTICS

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT-III 4-TERMINAL MOSFET

Threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT-IV SUB-THRESHOLD CURRENT MODELS

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT-V SOI MOSFET

Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.

2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009.

COURSE OUTCOMES:

1. Understand the physics of 2-terminal MOS operation and its characteristics
2. Understand the concept of MOS capacitor.
3. Understand the physics of 4-terminal MOSFET operation and its characteristics.
4. To understand Sub threshold current model.
5. Analyze the SOI MOSFET electrical characteristics

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

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L	T	P	C
3	0	0	3

(25D57104E) MICROELECTRONIC: DEVICE TO CIRCUITS (PE-II)

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To introduce the fundamental principles and operation of semiconductor devices used in analog and digital electronic circuits.
2. To develop the ability to analyze and design basic electronic circuits using diodes, BJTs, and MOSFETs.
3. To explain the characteristics and applications of amplifier and switching circuits in both discrete and integrated forms.
4. To provide understanding of frequency response, feedback, and stability aspects in analog circuit design.
5. To enable students to integrate analog and digital concepts for designing mixed-signal electronic systems

UNIT-I TRANSISTOR FUNDAMENTALS AND BASIC CIRCUIT MODELS

Bipolar Junction Transistor; Physical Structure and Modes of operation, Operation in Active Mode, circuit symbols and conventions, BJT as an Amplifier, small circuit model, BJT as a switch and Ebers Moll Model, Simple BJT inverter and Second Order Effects. MOS Transistor Basic, MOS Parasitic & SPICE Model; CMOS Inverter Basics-I

UNIT-II MOS AND BJT AMPLIFIER DESIGN

Power Analysis SPICE Simulation-I**,** Biasing of MOS Amplifier and its behavior as an analog switch, CMOS CS/CG/SF Amplifier Configuration, Internal cap models and high frequency modelling, JFET, structure and operation. Multistage and Differential Amplifier, Small Signal Operation and Differential Amplifier, MOS Differential Amplier, BiCMOS Amplifier with Active Load, Multistage Amplifier with SPICE Simulation

UNIT-III FREQUENCY RESPONSE AND FEEDBACK IN AMPLIFIERS

S-domain analysis, transfer function, poles and zeros, High Frequency Response of CS and CE Amplifier, Frequency Response of CC and SF Configuration, Frequency Response of the Differential Amplifier, Cascode Connection and its Operation. General Feedback structure and properties of negative feedback, Basic Feedback Topologies, Design of Feedback Amplifier for all configuration, Stability and Amplifier poles, Bode Plots and Frequency Compensation

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UNIT-IV OPERATIONAL AMPLIFIERS AND ANALOG FILTERS

Ideal Operational Amplifier and its terminals, Inverting and Non- Inverting Configuration, As an integrator and Differentiator, Introduction to Analog Computer, Large Signal Operation of Op-Amp and Second order offsets. Butterworth and Chebyshev Filters, First and Second Order Filter Functions, Switched Capacitor based filters, Single-Amplifier Biquadratic Filters, Second Order LCR Resonator.

UNIT-V DIGITAL LOGIC AND SEQUENTIAL CIRCUIT DESIGN

Combinational Logic Design, Sequential Logic Design, Clock Strategies for Sequential Design, Concept of Memory & its Designing

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009.

COURSE OUTCOMES:

1. Explain the working principles of semiconductor devices and their roles in electronic circuits.
2. Analyze the performance of analog and digital circuits using appropriate circuit theorems and models.
3. Design and implement amplifier, oscillator, and switching circuits meeting specified requirements.
4. Evaluate the effects of feedback, frequency response, and biasing on circuit stability and performance.
5. Apply learned concepts to design and simulate discrete and integrated circuits used in practical electronic systems.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

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L	T	P	C
0	0	4	2

(25D57105) CMOS ANALOG IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. To explain the Physical Verification in Layout Design
4. To fully appreciate the design and analyze of analog and mixed signal simulation
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments

1. MOS Device Characterization and parametric analysis

2. Common Source Amplifier

3. Common Source Amplifier with source degeneration

4. Cascode amplifier

5. Simple current mirror

6. Cascode current mirror.

7. Wilson current mirror.

8. Differential Amplifier

9. Operational Amplifier

10. Sample and Hold Circuit

11. Direct-conversion ADC

12. R-2R Ladder Type DAC

The students are required to design and implement any TEN Experiments using CMOS 130nm Technology.

The students are required to implement LAYOUTS of any SIX Experiments using CMOS

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130nm Technology and Compare the results with Pre-Layout Simulation.

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using VLSI design tool.
2. Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. Explain the Physical Verification in Layout Design
4. Fully appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									

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M.Tech. I Sem.

L	T	P	C
0	0	4	2

(25D57106) CMOS DIGITAL IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

1. **Inverter Characteristics.**
2. **NAND and NOR Gate**
3. **XOR and XNOR Gate**
4. **2:1 Multiplexer**
5. **Full Adder**
6. **RS-Latch**
7. **Clock Divider**
8. **JK-Flip Flop**
9. **Synchronous Counter**
10. **Asynchronous Counter**
11. **Static RAM Cell**
12. **Dynamic Logic Circuits**
13. **Linear Feedback Shift Register**

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using any VLSI design tool
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Explain the Physical Verification in Layout Extraction
4. Fully appreciate the design and analyze of CMOS Digital Circuits
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									

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CO3									
CO4									
CO5									

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M.Tech. I Sem.

L	T	P	C
2	0	0	2

(25D57107) RESEARCH METHODOLOGY AND IPR

Course Category	**Mandatory Course (credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the research design process and data collection methods.
2. To develop skills in data analysis and reporting.
3. To familiarize students with intellectual property rights (IPR) and patents.
4. To apply research skills in real-world contexts.

UNIT-I FUNDAMENTALS OF RESEARCH METHODOLOGY

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

Learning Outcomes

- Recall key concepts of the research process, including different types and approaches to research, and the importance of ethics.
- Differentiate between qualitative and quantitative research approaches and the various uses of secondary data.
- Identify the core principles of research design and ethics, including plagiarism and documentation styles.
- Explain the significance of reasoning and ethical conduct in all stages of the research process.

Apply knowledge of different documentation styles, such as APA and IEEE, to properly cite sources and avoid plagiarism.

UNIT-II DATA COLLECTION AND SOURCES

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

Learning Outcomes

- Identify different types of data and the various methods for collecting both primary and secondary data.
- Explain the importance of data quality and ethical considerations in data collection.
- Differentiate between primary, secondary, and Big Data sources.
- Describe the various tools and technologies used for effective data collection.

Analyze the ethical implications of data collection and ensure data quality in a research study.

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UNIT-III DATA ANALYSIS AND REPORTING

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

Learning Outcomes

- Apply knowledge of multivariate analysis and experimental research to develop hypotheses and analyze data.
- Explain the process of measurement systems analysis and error propagation in experimental design.
- Formulate clear and concise abstracts, introductions, and methodologies for research papers.
- Write effective results and discussion sections based on data analysis.

Develop comprehensive research papers and proposals based on proper data analysis and reporting guidelines.

UNIT-IV UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Learning Outcomes

- Recall the fundamental concepts of Intellectual Property (IP) and its evolution.
- Describe the roles of organizations like **WIPO** and **WTO** in the establishment of IPR.
- Differentiate between various types of IPR, including trade secrets and trademarks.
- Explain the common rules and features of IPR agreements and the role of UNESCO.

Analyze the relationship between IPR and biodiversity, and its broader impact.

UNIT-V PATENTS

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Learning Outcomes

- Explain the objectives, benefits, and key features of a patent, including the concept of an inventive step.
- Differentiate between the various types of patent applications and the e-filing process.
- Describe the process of patent examination, grant, and revocation.
- Identify the roles of patent agents and the process for their registration.

Analyze the concepts of equitable assignments, licenses, and licensing of related patents.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004

2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

REFERENCE BOOKS:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.
6. Peter Elbow, Writing With Power, Oxford University Press, 1998.

e-Resources and Digital Material:

1. Coursera / edX – Research Methodology and Data Analysis courses
2. Springer Link & ScienceDirect – Latest journals on research design and statistics
3. Google Scholar – Free access to research papers
4. NCBI Bookshelf – Open-access research methodology resources
5. Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

COURSE OUTCOMES:

1. Recall key concepts and terminology related to research design, data collection, and intellectual property rights.
2. Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.
3. Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.
4. Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.
5. Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods. 6. Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									

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CO3									
CO4									
CO5									

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L	T	P	C
0	1	2	2

(25D57108) RTL SYNTHESIS, SIMULATION AND VERIFICATION

Course Category	**Skill Oriented Course (SC)**
Course Enrichment Relevance	**Skill Development**

COURSE OBJECTIVES:

1. The simulation of combinational and sequential circuits.
2. FSM based designs.
3. Implementation of DFT and FFTs.
4. Verify layout of basic digital circuits.

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (SystemVerilog/VHDL basics).
- Lab:

1. Write synthesizable Verilog/SystemVerilog code for:

   a) Half Adder, Full Adder

   b) 4-bit Ripple Carry Adder

   c) 4-bit Synchronous Counter (Up/Down)

2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:

1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool

2. Generate gate-level netlist and analyze area, delay, power reports.

3. Apply constraints (clock, timing) and observe impact on synthesis

results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations

1. Develop testbenches for:
   a) 4-bit ALU (add, sub, AND, OR).
   b) Universal Shift Register.
2. Perform functional simulation using EDA tools
3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.

1. Write self-checking testbenches for combinational and sequential circuits.
2. Use assertion-based verification (SystemVerilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:

1. UART Transmitter/Receiver
2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)

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3. FIFO Buffer with full/empty flags

TEXT BOOKS:

1. Samir Palanitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Pearson, 2007.
2. Michael Ciletti – Advanced Digital Design with the Verilog HDL.
3. Chris Spear & Greg Tumbush – SystemVerilog for Verification.
4. David Rich – Design and Verification with SystemVerilog.
5. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.
6. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.

e-Resources and Digital Material:

COURSE OUTCOMES:

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs.
5. Build and verify various digital circuits.4. Employ simulation and formal verification methodologies, including assertion-based verification and equivalence checking.
6. Integrate RTL modules and perform case-study designs covering hierarchical design, DFT, HLS, and FPGA implementation.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									
CO6									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109A) ENGLISH FOR RESEARCH PAPER WRITING (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To equip students with the fundamentals of academic English for research paper writing.
2. To develop students' advanced reading skills for analyzing and evaluating research articles.
3. To refine students' grammar and language skills for clarity and precision in research writing.
4. To master the skills of revising, editing, and proofreading research papers.
5. To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.

UNIT-I FUNDAMENTALS OF ACADEMIC ENGLISH

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT-II READING SKILLS FOR RESEARCHERS

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT-III GRAMMAR REFINEMENT FOR RESEARCH WRITING

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT-IV MASTERY IN REFINING WRITTEN CONTENT/EDITING SKILLS

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

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UNIT-V TECHNOLOGY AND LANGUAGE FOR RESEARCH

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

TEXT BOOKS:

1. Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge,2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

REFERENCE BOOKS:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007
3. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005
4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R.Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R.How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

e-Resources and Digital Material:

1. https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/
2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview
3. Writing in the Sciences" – Stanford University (MOOC on Coursera) https://www.coursera.org/learn/sciwrite
4. Academic Phrasebank – University of Manchester http://www.phrasebank.manchester.ac.uk
5. OWL (Online Writing Lab) – Purdue University, https://owl.purdue.edu *(Resources on APA/MLA formats, grammar, structure, paraphrasing)*
6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources

COURSE OUTCOMES:

1. Recall the key language aspects and structural elements of academic writing in research papers.
2. Explain the importance of clarity, precision, and objectivity in research writing.
3. Apply critical reading strategies and advanced grammar skills to analyze and write research papers.

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4. Analyze research articles and identify the strengths and limitations of different methodologies.
5. Evaluate research papers to check for plagiarism, structure, clarity, and language accuracy.
6. Evaluate the effectiveness of different language and technology tools in research writing, including AI-assisted tools and plagiarism detection software and Develop a well-structured research paper that effectively communicates complex ideas.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									
CO6									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109B) VALUE EDUCATION (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

UNIT-I VALUES AND SELF-DEVELOPMENT

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II IMPORTANCE OF VALUES

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III PERSONALITY AND BEHAVIOR DEVELOPMENT

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV AVOID FAULT THINKING

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V CHARACTER AND COMPETENCE

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

COURSE OUTCOMES:

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

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Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109C) DISASTER MANAGEMENT (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Environment & Sustainability**

COURSE OBJECTIVES:

1. To enable the students to understand the fundamental concepts of disasters, hazards, their factors, and significance with special reference to India.
2. To prepare them to classify and analyze different types of natural and man-made disasters, their causes, magnitude, and impacts.
3. To foster them develop understanding of disaster preparedness, monitoring systems, and the role of government, community, and media.
4. To equip them in learning risk assessment techniques, disaster risk reduction strategies, and the importance of global and national cooperation. 5. To foster their ability to think critically and respond to disasters and design effective mitigation measures (structural and non-structural) with a focus on emerging trends and Indian disaster management programs.

UNIT-I INTRODUCTION & DISASTER PRONE AREAS IN INDIA

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude. Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT-II REPERCUSSIONS OF DISASTERS AND HAZARDS

Economic Damage - Loss of Human and Animal Life - Destruction of Ecosystem - Natural Disasters - Earthquakes, Volcanism, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster - Nuclear Reactor Meltdown - Industrial Accidents - Oil Slick sand Spills - Outbreaks of Disease and Epidemics War and Conflicts

UNIT-III DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness - Monitoring of Phenomena - Triggering a Disasteror Hazard - Evaluation of Risk-Application of Remote Sensing - Data from Meteorological and Other Agencies - Media Reports- Governmental and Community Preparedness

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UNIT-IV RISK ASSESSMENT DISASTER RISK

Disaster Risk -Concept and Elements, Disaster Risk Reduction - Global and National Disaster Risk Situation -Techniques of Risk Assessment – Global Co-Operation in Risk Assessment and Warning - People's participation in Risk Assessment – Strategies for Survival

UNIT-V DISASTER MITIGATION

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS:

1. Gupta, H. K. Disaster Management. Universities Press, 2003
2. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.

REFERENCE BOOKS:

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.
4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.
5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

e-Resources and Digital Material:

1. National Disaster Management Authority (NDMA), India: https://ndma.gov.in – official guidelines, reports, and policy frameworks.
2. United Nations Office for Disaster Risk Reduction (UNDRR): https://www.undrr.org – Sendai Framework, global risk reduction strategies.
3. Global Disaster Alert and Coordination System (GDACS): https://www.gdacs.org – real-time disaster alerts.
4. World Health Organization (WHO) – https://www.who.int/emergencies – disaster-related health guidelines.

COURSE OUTCOMES:

1. Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.

2. Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters.
3. Assess the economic, social, and ecological repercussions of major natural and man-made disasters.
4. Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.
5. Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.
6. Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									
CO6									

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(25D57109D) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE (AC-I)

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

1. To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.
2. To make them understand the need for protecting traditional knowledge and its significance in the global economy.
3. To make them understand the legal frame work and policies related to traditional knowledge protection.
4. To enable them to understand the relationship between traditional knowledge and intellectual property rights.
5. To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

UNIT-I INTRODUCTION TO TRADITIONAL KNOWLEDGE

Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge - Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge.

UNIT-II PROTECTION, NEED, SIGNIFICANCE, VALUE AND ROLE OF TRADITIONAL KNOWLEDGE

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK

UNIT-III LEGAL FRAME WORK

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

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UNIT-IV TRADITIONAL KNOWLEDGE AND INTELLECTUAL PROPERTY

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT-V TRADITIONAL KNOWLEDGE IN DIFFERENT SECTORS

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TKTraditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

TEXT BOOKS:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh,Traditional Knowledge System and Technology in India, PratibhaPrakashan 2012.

REFERENCE BOOKS:

1. Pride of India: A Glimpse into India’s Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. “On Astronomy in Ancient India”, Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

e-Resources and Digital Material:

1. https://www.youtube.com/watch?v=LZP1StpYEPM
2. http://nptel.ac.in/courses/121106003/

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Define and explain the concept of traditional knowledge, its nature, characteristics, and scope
2. Understand the need for protecting traditional knowledge and its significance in the global economy
3. Explain the legal framework and policies related to traditional knowledge protection
4. Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology
5. Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change
6. Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms

Mapping COs with POs & PSOs:

CO/PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
CO1									
CO2									
CO3									
CO4									
CO5									
CO6									

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VISION

- To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

MISSION

M1: To provide Advanced Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization by arising a self-sustained University.

M2: To establish postgraduate programs in the current and Advanced Technologies.

M3: To establish an R&D Consultancy through developing Industry Institute Interaction, building up exceptional infrastructure.

M4: To propel every individual, realize and act for the technical development of the society

MOTTO

- Education for Peace and Progress

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